16Gb NAND FLASH

HY27UU08AG(5/D)A
HY27UU08AG5A
HY27UU08AGDA

Document Title
16Gbit (2Gx8bit) NAND Flash Memory

Revision History

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<tr><td>0.0</td><td>Initial Draft.</td><td>May. 18. 2007</td><td>Preliminary</td></tr>
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FEATURES SUMMARY

HIGH DENSITY NAND FLASH MEMORIES
- Cost effective solutions for mass storage applications

MULTIPLANE ARCHITECTURE
- Array is split into two independent planes. Parallel Operations on both planes are available, halving Program and erase time.

NAND INTERFACE
- x8 bus width
- Multiplexed address/ Data
- Pinout compatibility for all densities

SUPPLY VOLTAGE
-3.3V device : Vcc = 2.7 V ~3.6 V

MEMORY CELL ARRAY
- (2k + 64) bytes x 128 pages x 8192 blocks

PAGE SIZE
- x8 device : (2048+64 spare) bytes
  : HY27UU08AG(5/D)A

BLOCK SIZE
- x8 device : (256K+8K) bytes

PAGE READ / PROGRAM
- Random access: 60us (Max)
- Sequential access: 25ns (Min)
- Page program time: 800us (Typ)
- Multi-Plane page program time : 800us (Typ)

COPY BACK PROGRAM
-Fast page copy

FAST BLOCK ERASE
- Block erase time: 2.5ms (Typ)
- Multi-Plane block erase time (2blocks) : 2.5ms(Typ)

STATUS REGISTER

ELECTRONIC SIGNATURE
- 1st cycle: Manufacturer Code
- 2nd cycle: Device Code
- 3th cycle: Internal chip number, Cell Type, Number of Simultaneously Programmed Pages.
- 4th cycle: Page size, Block size, Organization, Spare size
- 5th cycle: Multiplane information

CHIP ENABLE DON'T CARE
-Simple interface with microcontroller

HARDWARE DATA PROTECTION
- Program/Erase locked during Power transitions.

DATA RETENTION
- 10000 Program / Erase cycles (with 4bit/528byte ECC)
- 10 Years Data Retention

PACKAGE
- HY27UU08AG5A-T(P)
  : 48-pin TSOP1(12 x 20 x 1.2 mm)
    - HY27UU08AG5A-T (Lead)
    - HY27UU08AG5A-TP (Lead Free)

- HY27UU08AGDA-UP
  : 52-ULGA (12 x 17 x 0.65 mm)
    - HY27UU08AGDA-DT (Lead Free)

1.SUMMARY DESCRIPTION

The HY27UU08AG(5/D)A is a 2048Mx8bit with spare 64Mx8 bit capacity. The device is offered in 3.3V Vcc Core Power Supply, 3.3V Input-Output Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.
The device contains 8192 blocks, composed by 128 pages consisting in two NAND structures of 32 series connected Flash cells. Every cell holds two bits. Like all other 2KB page NAND Flash devices, a program operation allows to write the 2112-byte page in typical 800us and an erase operation can be performed in typical 2.5ms on a 256K-byte block.
In addition to this, thanks to multiplane architecture, it is possible to program 2 pages a time (one per each plane) or to erase 2 blocks a time (again, one per each plane). As a consequence, multiplane architecture allows program time reduction by 47% and erase time reduction by 50%. Data in the page can be read out at 25ns cycle time per byte.
The I/O pins serve as the ports for address and data input/output as well as command input.
This interface allows a reduced pin count and easy migration towards different densities, without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using CE, WE, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data. The modify operations can be locked using the WP Input.
The output pin R/B (open drain buffer) signals the status of the device during each operation.
In a system with multiple memories the R/B pins can be connected all together to provide a global status signal.
Even the write-intensive systems can take advantage of the HY27UU08AG(5/D)A extended reliability of 10K program/ erase cycles by providing ECC (Error Correcting Code) with real time mapping-out algorithm.
The chip supports CE don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE transitions do not stop the read operation.
This device includes also extra Features like OTP/Unique ID area, Read ID2 extension.
The HY27UU08AG(5/D)A is available in 48 - TSOP1 12 x 20 mm, 52 - ULGA 12x17 mm package.

1.1 Product List

PART NUMBER	ORGANIZATION	Vcc RANGE	PACKAGE
HY27UU08AG5A	x8	2.7~3.6 Volt	48TSOP1
HY27UU08AGDA			52-ULGA

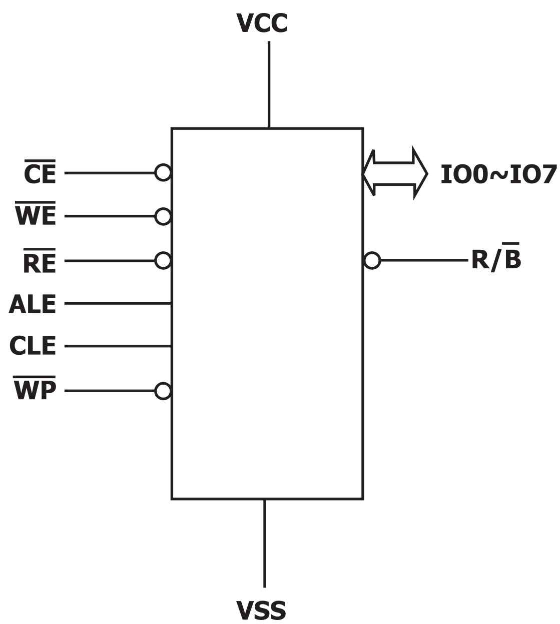


Figure1: Logic Diagram

IO7 - IO0	Data Input / Outputs
CLE	Command latch enable
ALE	Address latch enable
$\overline{CE}$1, $\overline{CE}$2	Chip Enable
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
R/$\overline{B}$1, R/$\overline{B}$2	Ready / Busy
Vcc	Power Supply
Vss	Ground
NC	No Connection

Table 1: Signal Names

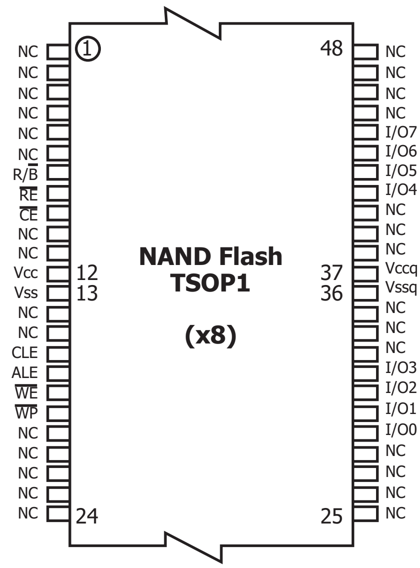


Figure 2. 48TSOP1 Contact, x8 Device

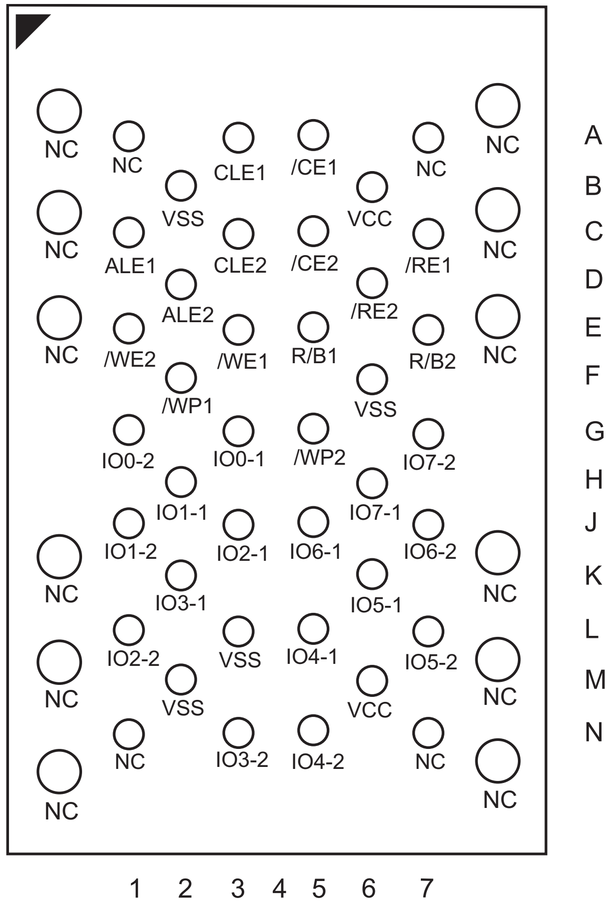


Figure 3. 52-ULGA Contactions, x8 Device, Dual interface
(Top view through package)

1.2 PIN DESCRIPTION

Pin Name	Description
IO0-IO7	**DATA INPUTS/OUTPUTS** The IO pins allow to input command, address and data and to output data during read / program operations. The inputs are latched on the rising edge of Write Enable ($\overline{WE}$). The I/O buffer float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the IO inputs inside the Command Register on the Rising edge of Write Enable ($\overline{WE}$).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the IO inputs inside the Address Register on the Rising edge of Write Enable ($\overline{WE}$).
$\overline{CE1}$, $\overline{CE2}$	**CHIP ENABLE** This input controls the selection of the device. When the device is busy $\overline{CE1}$, $\overline{CE2}$ low does not deselect the memory.
$\overline{WE}$	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The IO inputs are latched on the rise edge of $\overline{WE}$.
$\overline{RE}$	**READ ENABLE** The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.
$\overline{WP}$	**WRITE PROTECT** The $\overline{WP}$ pin, when Low, provides an Hardware protection against undesired modify (program / erase) operations.
R/$\overline{B1}$, R/$\overline{B2}$	**READY BUSY** The R/$\overline{B1}$, R/$\overline{B2}$ output is an Open Drain pin that signals the state of the memory.
Vcc	**SUPPLY VOLTAGE** The Vcc supplies the power for all the operations (Read, Write, Erase).
Vss	GROUND
NC	NO CONNECTION

Table 2: Pin Description

NOTE:

1. A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th Cycle	A28	A29	A30	L(1)	L(1)	L(1)	L(1)	L(1)

Table 3: Address Cycle Map(x8)

NOTE:
1. L must be set to Low.

FUNCTION	1st CYCLE	2nd CYCLE	3rd CYCLE	4th CYCLE	Acceptable command during busy
PAGE READ	00h	30h	-		
READ FOR COPY-BACK	00h	35h	-		
READ ID	90h	-	-		
RESET	FFh	-	-		Yes
PAGE PROGRAM	80h	10h	-		
MULTI PLANE PAGE PROGRAM	80h	11h	81h	10h	
COPY BACK PGM	85h	10h	-		
MULTI PLANE COPYBACK PROGRAM	85h	11h	81h	10h	
BLOCK ERASE	60h	D0h	-		
MULTI PLANE BLOCK ERASE	60h	60h	D0h		
READ STATUS REGISTER	70h	-	-		Yes
RANDOM DATA INPUT	85h	-	-		
RANDOM DATA OUTPUT	05h	E0h	-		

Table 4: Command Set

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input(5 cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H	L	Rising	H	H		Address Input(5 cycles)
L	L	L	Rising	H	H	Data Input	
L	L	L(1)	H	Falling	X	Sequential Read and Data Output	
L	L	L	H	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc	Stand By	

Table 5: Mode Selection

NOTE:

1. With the $\overline{CE}$ high during latency time does not stop the read operation

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.
Typically glitches less than 3 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1 Command Input.

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See figure 5 and table 12 for details of the timings requirements. Command codes are always applied on IO7:0, disregarding the bus configuration.

2.2 Address Input.

Address Input bus operation allows the insertion of the memory address. Five cycles are required to input the addresses for the 16Gbit devices. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable high and latched on the rising edge of Write Enable. Moreover for commands that starts a modifying operation (write/erase) the Write Protect pin must be high. See figure 6 and table 12 for details of the timings requirements. Addresses are always applied on IO(7:0), disregarding the bus configuration.
In addition, addresses over the addressable space are disregarded even if the user sets them during command insertion.

2.3 Data Input.

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See figure 7 and table 12 for details of the timings requirements.

2.4 Data Output.

Data Output bus operation allows to read data from the memory array and to check the status register content, the ID data. Data can be serially shifted out toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See figures 8,9,11,12,13 and table 12 for details of the timings requirements.

2.5 Write Protect.

Hardware Write Protection is activated when the Write Protect pin is low. In this condition modify operation does not start and the content of the memory is not altered. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.

2.6 Standby

In Standby mode the device is deselected, outputs are disabled and Power Consumption is reduced. Stand-by is obtained holding high, at least for 10us, $\overline{CE}$ pin.

3. DEVICE OPERATION

3.1 Page Read.

Page read operation is initiated by writing 00h and 30h to the command register along with five address cycles.
In two consecutive read operaions, the second one need 00h command, which five address cycles and 30h command initiates that operation.
Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 2112 bytes of data within the selected page are transfered to the data registers in less than 60us(tR). The system controller may detect the completion of this data transfer 60us(tR) by analyzing the output of R/$\overline{B}$ pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing RE. The repetitive high to low transitions of the RE clock make the device output the data starting from the selected column address up to the last column address. The device may output random data in a page instead of the consecutive sequential data by writing random data output command.
The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.

3.2 Page Program.

The device is programmed by page. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 1 times. The addressing should be done on each pages in a block. A page program cycle consists of a serial data loading period in which up to 2112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The bytes other than those to be programmed do not need to be loaded. The device supports random data input in a page.
The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/$\overline{B}$ output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s.
The command register remains in Read Status command mode until another valid command is written to the command register. Figure 14 details the sequence.

3.3 Multi Plane Program.

Device supports multiple plane program: it is possible to program in parallel 2 pages, one per each plane.
A multiple plane program cycle consists of a double serial data loading period in which up to 4224bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data for the 1st page. Address for this page must be within 1st plane (A<19>=0). The data of 1st page other than those to be programmed do not need to be loaded. The device supports random data input exactly like page program operation. The Dummy Page Program Confirm command (11h) stops 1st page data input and the device becomes busy for a short time (tDBSY). Once it has become ready again, 81h command must be issued, followed by 2nd page address (5 cycles) and its serial data input. Address for this page must be within 2nd plane (A<19>=1). The data of 2nd page other than those to be programmed do not need to be loaded. Program Confirm command (10h) makes parallel programming of both pages start. User can check operation status by R/$\overline{B}$ pin or read status register command, as if it were a normal page program; status register command is also available during Dummy Busy time (tDBSY). In case of fail in 1st or 2nd page program, fail bit of status register will be set: Device supports pass/fail status of each plane (Table 13). (IO0 : Total, IO1: Plane0, IO2: Plane1). Figure 19 details the sequence.

3.4 Block Erase.

The Erase operation is done on a block basis. Block address loading is accomplished in there cycles initiated by an Erase Setup command (60h). Only address A19 to A30 is valid while A12 to A18 is ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal erasing process. This two step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify.
Once the erase process starts, the Read Status Register command may be entered to read the status register.
The system controller can detect the completion of an erase by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.
Figure 18 details the sequence.

3.5 Multi Plane Erase.

Multiple plane erase, allows parallel erase of two blocks, one per each memory plane.
Block erase setup command (60h) must be repeated two times, each time followed by 1st block and 2nd block address respectively (3 cycles each). As for block erase, D0h command makes embedded operation start. Multiplane erase does not need any Dummy Busy Time between 1st and 2nd block address insertion. Address limitation required for multiple plane program applies also to multiple plane erase, as well as operation progress can be checked like for multiple plane program through read status register (Table13). Figure 19 details the sequence

3.6 Copy-Back Program
Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored. Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register.
When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 16 & Figure 17). The command register remains in Read Status command mode until another valid command is written to the command register. During copy-back program, data modification is possible using random data input command (85h) as shown in Figure16.
Copy-back program operation is allowed only within same plane.

3.7 Multi-Plane Copy-Back Program
Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 2112 byte page registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte page registers enables a simultaneous programming of two pages. Figure 21 shows the command sequence for the multi plane copy-back operation.

3.8 Read Status Register.
The device contains a Status Register which may be read to find out whether, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 13 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

3.9 Read ID.
The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (ADh), and the device code and 3rd, 4th, 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 22 shows the operation sequence, while Table 15 explain the byte meaning.

3.10 Reset.
The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP is high. Refer to table 13 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted by the command register. The R/B pin goes low for tRST after the Reset command is written. Refer to Figure 25.

4. OTHER FEATURES

4.1 Data Protection & Power On/Off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever Vcc is below about 2.0V(3.3V device). $\overline{\text{WP}}$ pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences as shown in Figure 26. The two-step command sequence for program/erase provides additional software protection.

4.2 Ready/Busy.

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/$\overline{\text{B}}$ pin is normally high and goes to low when the device is busy (after a reset, read, program, erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/$\overline{\text{B}}$ outputs to be Or-tied.
Because pull-up resistor value is related to tR(R/$\overline{\text{B}}$) and current drain during busy (Ibusy), an appropriate value can be obtained with the following reference chart (Fig 27). Its value can be determined by the following guidance.

Parameter	Symbol	Min	Typ	Max	Unit
Valid Block Number	NVB	7992		8192	Blocks

Table 6: Valid Blocks Number

NOTE:

1. The 1st block is guaranteed to be a valid block at the time of shipment.

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (Commercial Temperature Range)	0 to 70	℃
	Ambient Operating Temperature (Industrial Temperature Range)	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	V
VIO(2)	Input or Output Voltage	-0.6 to 4.6	V
Vcc	Supply Voltage	-0.6 to 4.6	V

Table 7: Absolute maximum ratings

NOTE:

1. Except for the rating “Operating Temperature Range”, stresses above those listed in the Table “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the Hynix SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.

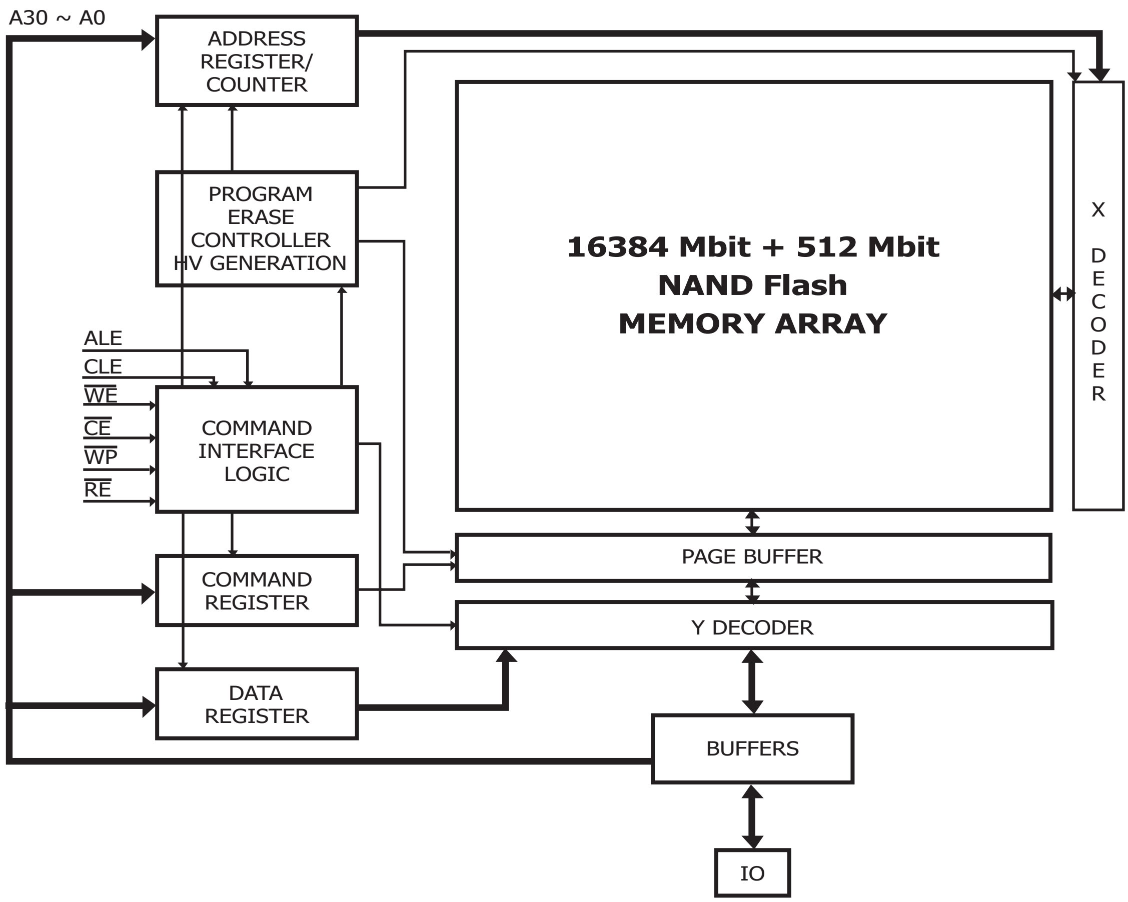


Figure 3: Block Diagram

Parameter		Symbol	Test Conditions	3.3Volt			Unit
				Min	Typ	Max	
Operating Current	Sequential Read	I_{CC1}	t_{RC}=25ns $\overline{CE}$=V_{IL}, I_{OUT}=0mA	-	15	30	mA
	Program	I_{CC2}	-	-	15	30	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (TTL)		I_{CC4}	$\overline{CE}$=V_{IH}, $\overline{WP}$=0V/Vcc	-		1	mA
Stand-by Current (CMOS)		I_{CC5}	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=0V/Vcc	-	20	100	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to Vcc (max)	-	-	± 20	uA
Output Leakage Current		I_{LO}	V_{OUT} =0 to Vcc (max)	-	-	± 20	uA
Input High Voltage		V_{IH}	-	0.8xVcc	-	Vcc+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xVcc	V
Output High Voltage Level		V_{OH}	I_{OH}=-400uA	2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
Output Low Current (R/$\overline{B}$)		I_{OL} (R/$\overline{B}$)	V_{OL}=0.4V	8	10	-	mA

Table 8: DC and Operating Characteristics

Parameter	Value
	3.3Volt
Input Pulse Levels	0V to VCC
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VCC/2
Output Load (2.7V - 3.6V)	1 TTL GATE and CL=50pF

Table 9: AC Conditions

Item	Symbol	Test Condition	Min	Max	Unit
Input / Output Capacitance	$C_{I/O}$	V_{IL}=0V	-	20	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	20	pF

Table 10: Pin Capacitance (TA=25C, F=1.0MHz)

Parameter	Symbol	Min	Typ	Max	Unit
Program Time / Multi-Plane Program Time	t_{PROG}	-	800	2000	us
Dummy Busy Time for Two Plane Program	t_{DBSY}	-	1	2	us
Number of partial Program Cycles in the same page	NOP	-	-	1	Cycles
Block Erase Time / Multi-Plane Block Erase Time	t_{BERS}	-	2.5	10	ms

Table 11: Program / Erase Characteristics

Parameter	Symbol	3.3V		Unit
		Min	Max	
CLE Setup time	t_{CLS}	12		ns
CLE Hold time	t_{CLH}	5		ns
$\overline{\text{CE}}$ setup time	t_{CS}	20		ns
$\overline{\text{CE}}$ hold time	t_{CH}	5		ns
$\overline{\text{WE}}$ pulse width	t_{WP}	12		ns
ALE setup time	t_{ALS}	12		ns
ALE hold time	t_{ALH}	5		ns
Data setup time	t_{DS}	12		ns
Data hold time	t_{DH}	5		ns
Write Cycle time	t_{WC}	25		ns
$\overline{\text{WE}}$ High hold time	t_{WH}	10		ns
Data Transfer from Cell to register	t_{R}		60	us
ALE to $\overline{\text{RE}}$ Delay	t_{AR}	10		ns
CLE to $\overline{\text{RE}}$ Delay	t_{CLR}	10		ns
Ready to $\overline{\text{RE}}$ Low	t_{RR}	20		ns
$\overline{\text{RE}}$ Pulse Width	t_{RP}	12		ns
$\overline{\text{WE}}$ High to Busy	t_{WB}		100	ns
Read Cycle Time	t_{RC}	25		ns
$\overline{\text{RE}}$ Access Time	t_{REA}		20	ns
$\overline{\text{RE}}$ High to Output High Z	t_{RHZ}		100	ns
$\overline{\text{CE}}$ High to Output High Z	t_{CHZ}		50	ns
$\overline{\text{CE}}$ High to Output hold	t_{COH}	15		ns
$\overline{\text{RE}}$ High to Output Hold	t_{RHOH}	15		ns
$\overline{\text{RE}}$ Low to Output Hold	t_{RLOH}	5		ns
$\overline{\text{RE}}$ High Hold Time	t_{REH}	10		ns
Output High Z to $\overline{\text{RE}}$ Low	t_{IR}	0		ns
$\overline{\text{CE}}$ Low to $\overline{\text{RE}}$ Low	t_{CR}	10		ns
Address to data loading time	t_{ADL}	70		ns
$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ low	t_{WHR}	80		ns
$\overline{\text{RE}}$ High to $\overline{\text{WE}}$ low	t_{RHW}	100		ns
Device Resetting Time (Read / Program / Erase)	t_{RST}		20/20/500(1)	us
Write Protection time	t_{WW}(2)	100		ns

Table 12: AC Timing Characteristics

NOTE:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us
2. Program / Erase Enable Operation : $\overline{\text{WP}}$ high to $\overline{\text{WE}}$ High.
   Program / Erase Disable Operation : $\overline{\text{WP}}$ Low to $\overline{\text{WE}}$ High.

IO	Pagae Program	Block Erase	Read	CODING
0	Pass / Fail	Pass / Fail	NA	Pass: ‘0’ Fail: ‘1’
1	Plane 0 Pass/Fail	Plane 0 Pass/Fail	NA	Plane 0, Pass : ‘0’ Fail : ‘1’
2	Plane 1 Pass/Fail	Plane 1 Pass/Fail	NA	Plane 1, Pass : ‘0’ Fail : ‘1’
3	NA	NA	NA	-
4	NA	NA	NA	-
5	NA	NA	NA	-
6	Ready/Busy	Ready/Busy	Ready/Busy	Busy: ‘0’ Ready’: ‘1’
7	Write Protect	Write Protect	Write Protect	Protected: ‘0’ Not Protected: ‘1’

Table 13: Status Register Coding

DEVICE IDENTIFIER CYCLE	DESCRIPTION
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, cell Type, etc.
4th	Page Size, Block Size, Spare Size, Organization
5th	Multiplane information

Table 14: Device Identifier Coding

Part Number	Voltage	Bus Width	1st cycle (Manufacture Code)	2nd cycle (Device Code)	3rd cycle	4th cycle	5th cycle
HY27UU08AG(5/D)A	3.3V	x8	ADh	D3h	14h	A5h	34h

Table 15: Read ID Data Table

	Description	IO7	IO6	IO5 IO4	IO3 IO2	IO1 IO0
Die / Package	1 2 4 8					0 0 0 1 1 0 1 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell				0 0 0 1 1 0 1 1	
Number of Simultaneously Programmed Pages	1 2 3 4			0 0 0 1 1 0 1 1		
Interleave Program Between multiple chips	Not Supported		0 1			
Write Cache	Not Supported	0 1				

Table 16: 3rd Byte of Device Idendifier Description

	Description	IO7	IO6	IO5-4	IO3	IO2	IO1-0
Page Size (Without Spare Area)	1KB 2KB 4KB 8KB						0 0 0 1 1 0 1 1
Spare Area Size (Byte / 512Byte)	8 16					0 1	
Serial Access Time	50ns 30ns 25ns Reserved	0 0 1 1			0 1 0 1		
Block Size (Without Spare Area)	64K 128K 256K 512KB			0 0 0 1 1 0 1 1			
Organization	X8 X16		0 1				

Table 17: 4th Byte of Device Idendifier Description

	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (w/o redundant Area)	512Mb		0	0	0				
	1Gb		0	0	1				
	2Gb		0	1	0				
	4Gb		0	1	1				
	8Gb		1	0	0				
	Reserved		1	0	1				
	Reserved		1	1	0				
	Reserved		1	1	1				
Reserved		0						0	0

Table 18: 5rd Byte of Device Idendifier Description

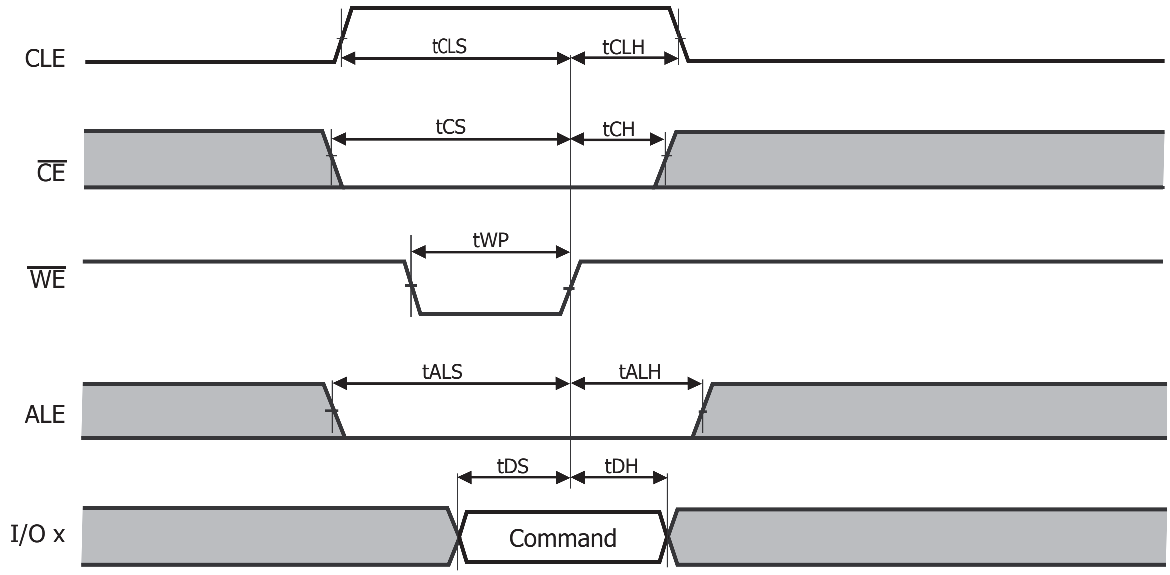


Figure 5: Command Latch Cycle

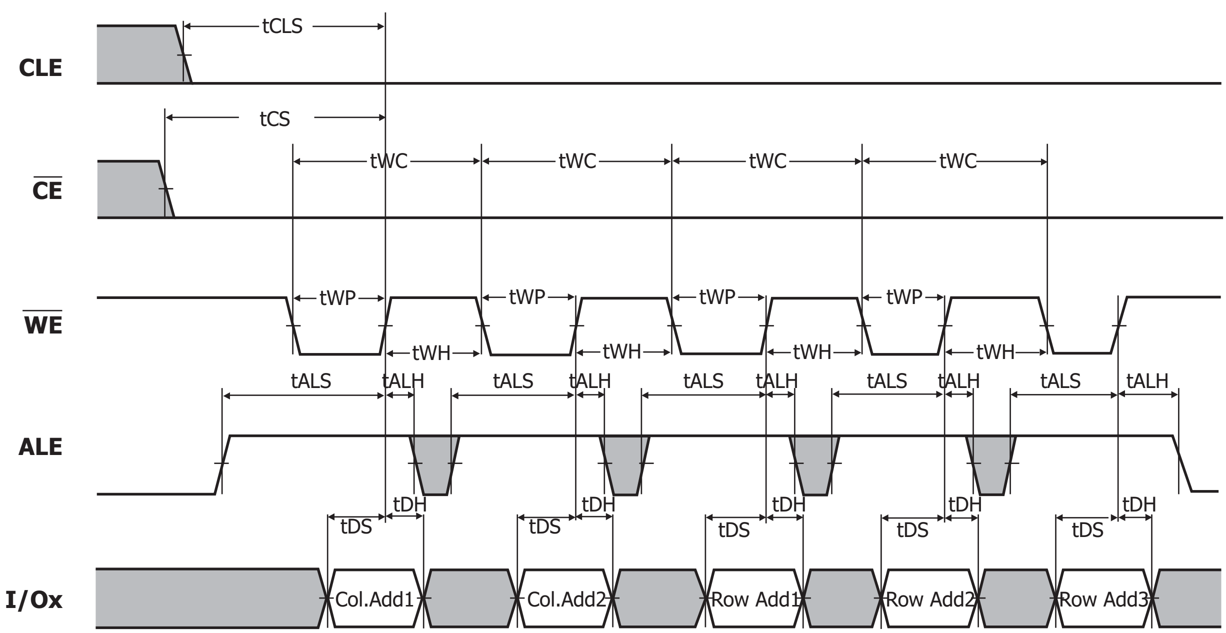


Figure 6: Address Latch Cycle

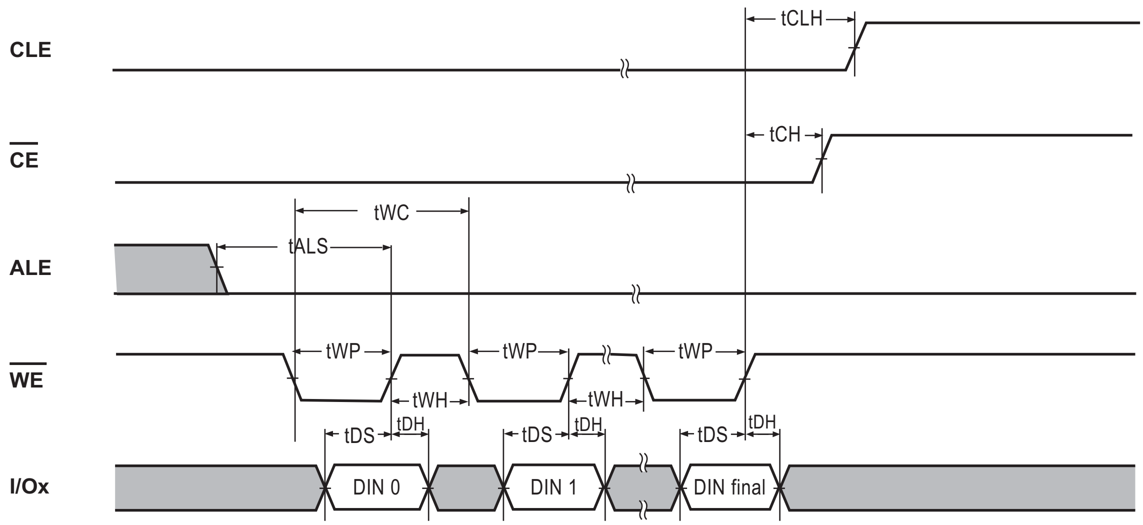
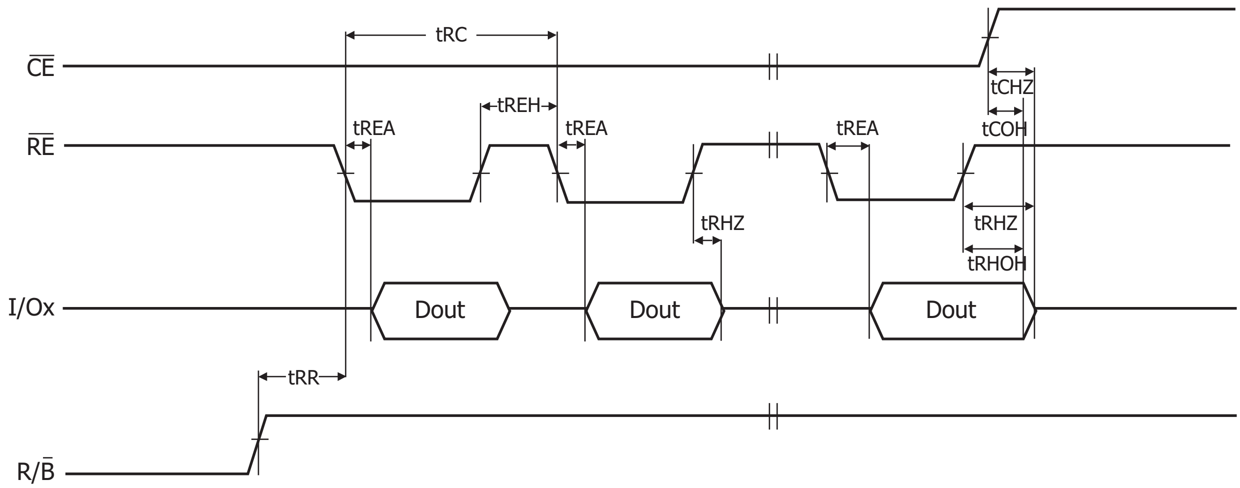
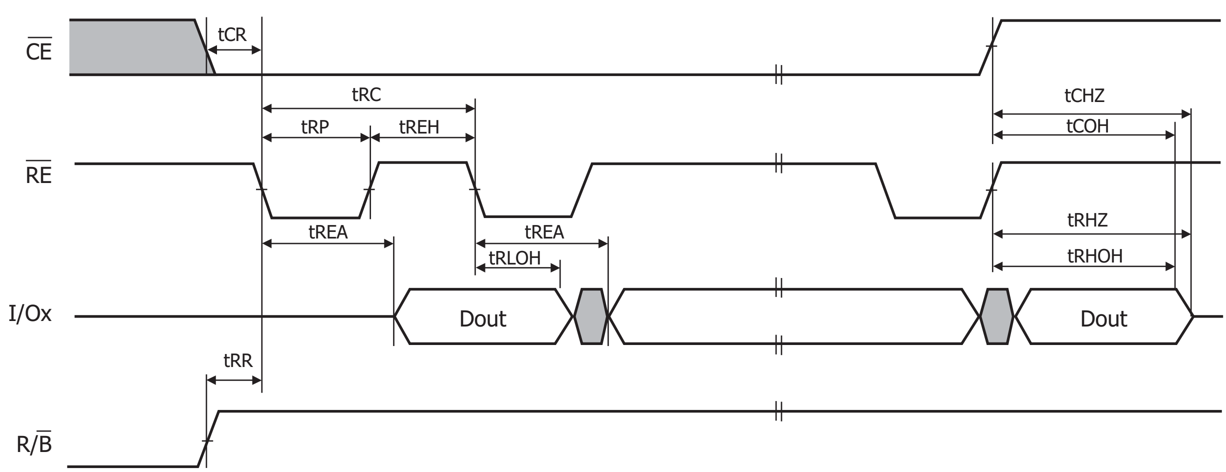


Figure 7. Input Data Latch Cycle



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 8: Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)



Notes: Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sampled and not 100% tested. (tCHZ, tRHZ)
tRLOH is valid when frequency is higher than 33MHz.
tRHOH starts to be valid when frequency is lower than 33MHz.

Figure 9: Sequential Out Cycle after Read (EDO Type CLE=L, $\overline{WE}$=H, ALE=L)

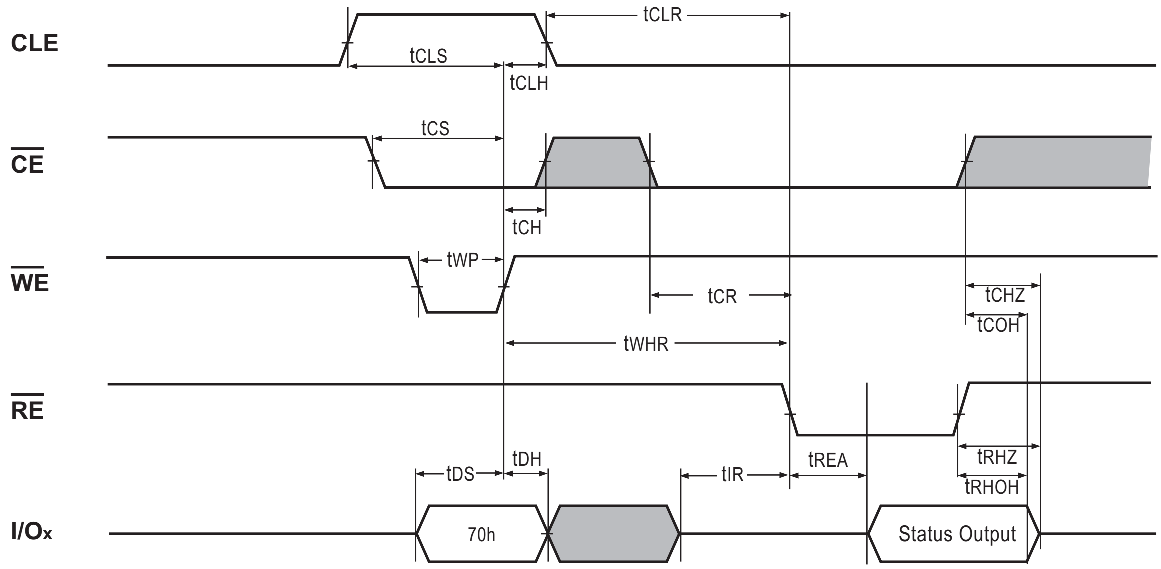


Figure 10: Status Read Cycle

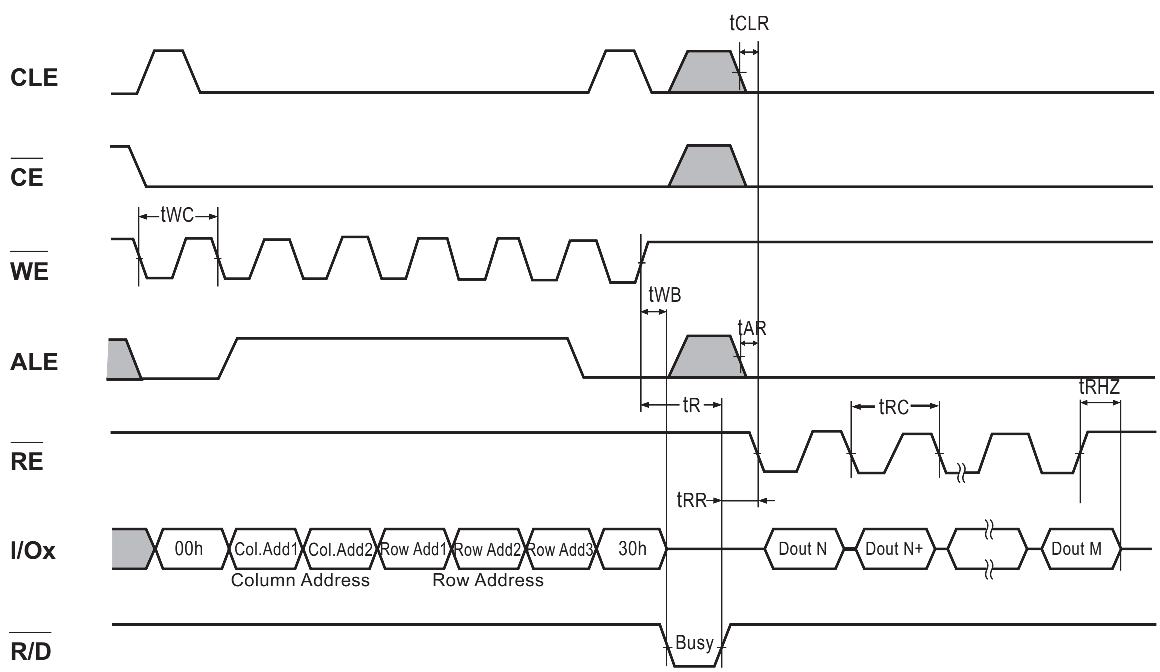


Figure 11: Read1 Operation (Read One Page)

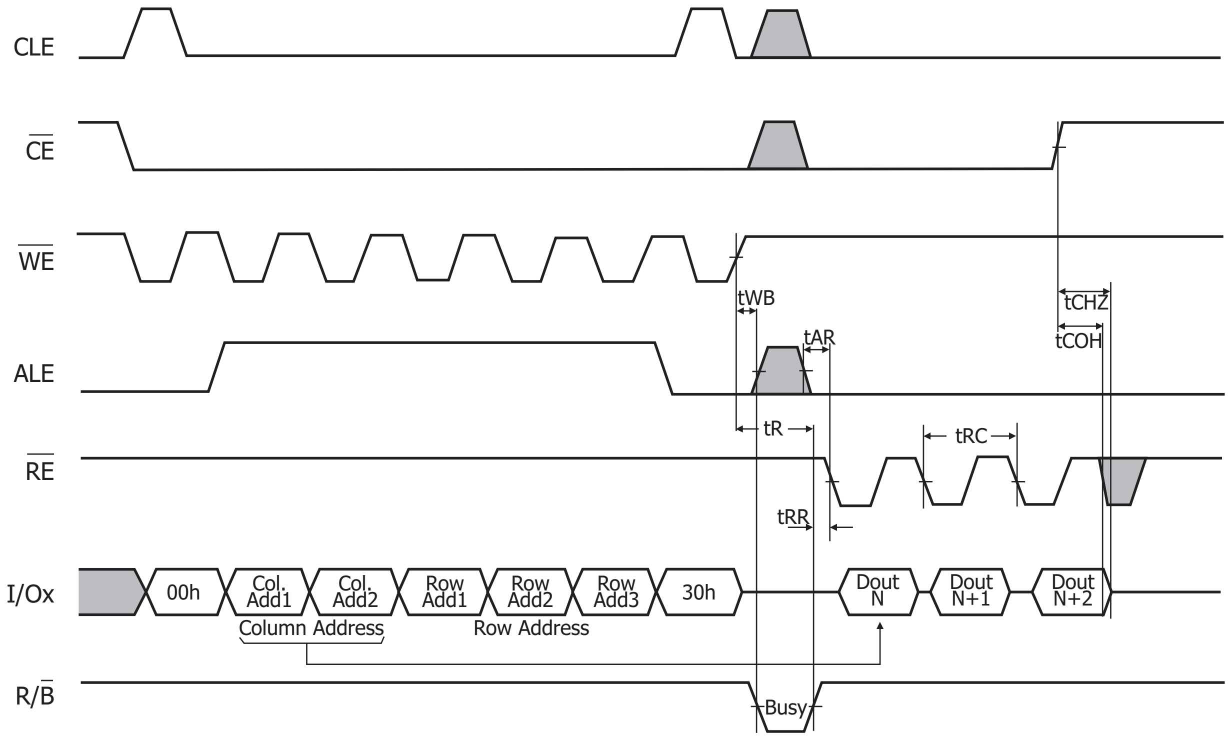


Figure 12: Read1 Operation intercepted by $\overline{CE}$

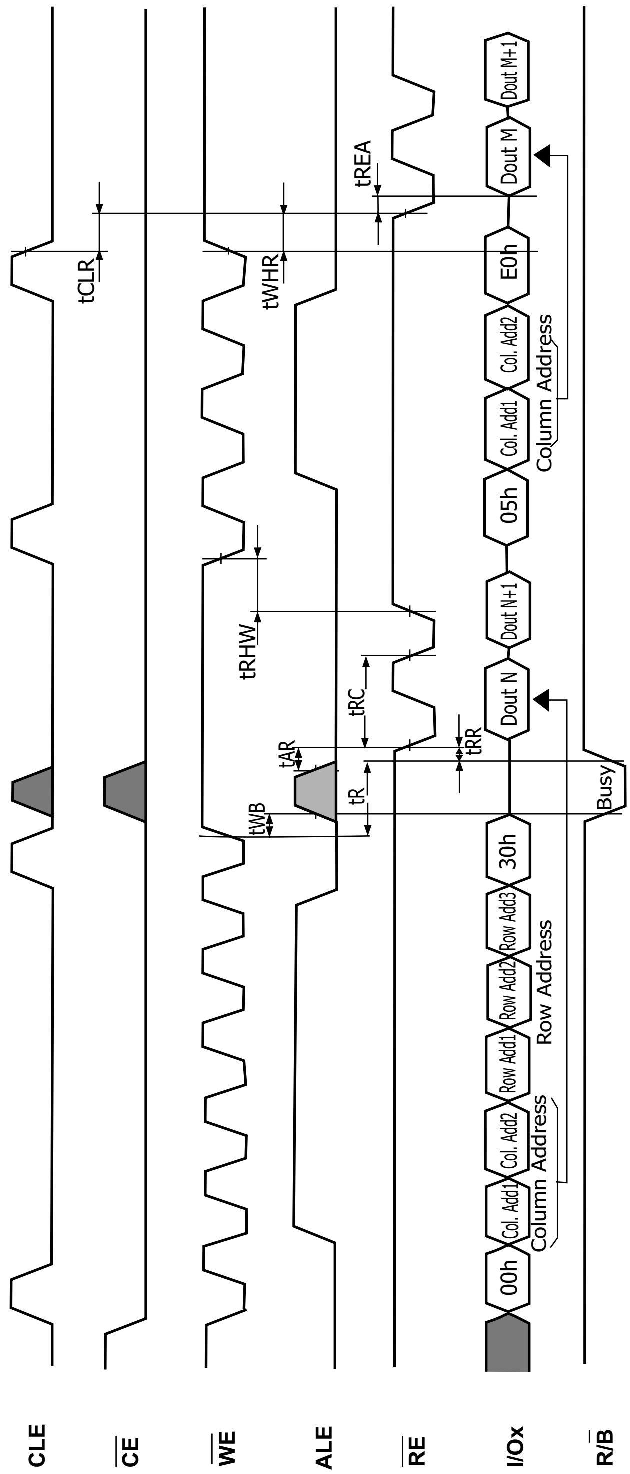
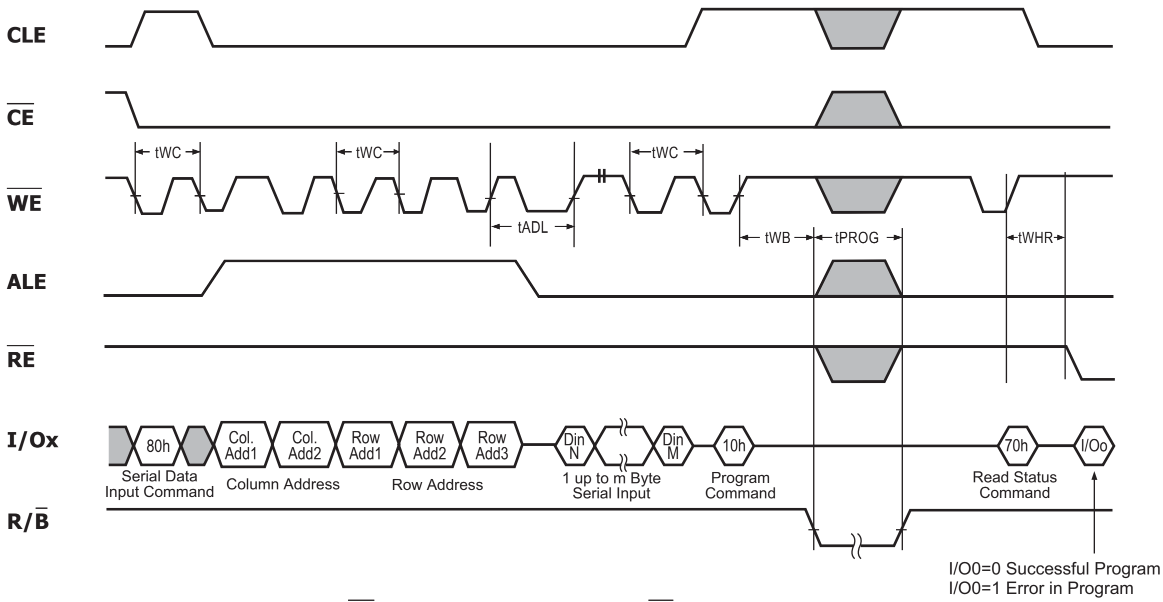


Figure 13 : Random Data output



NOTES : tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

Figure 14: Page Program Operation

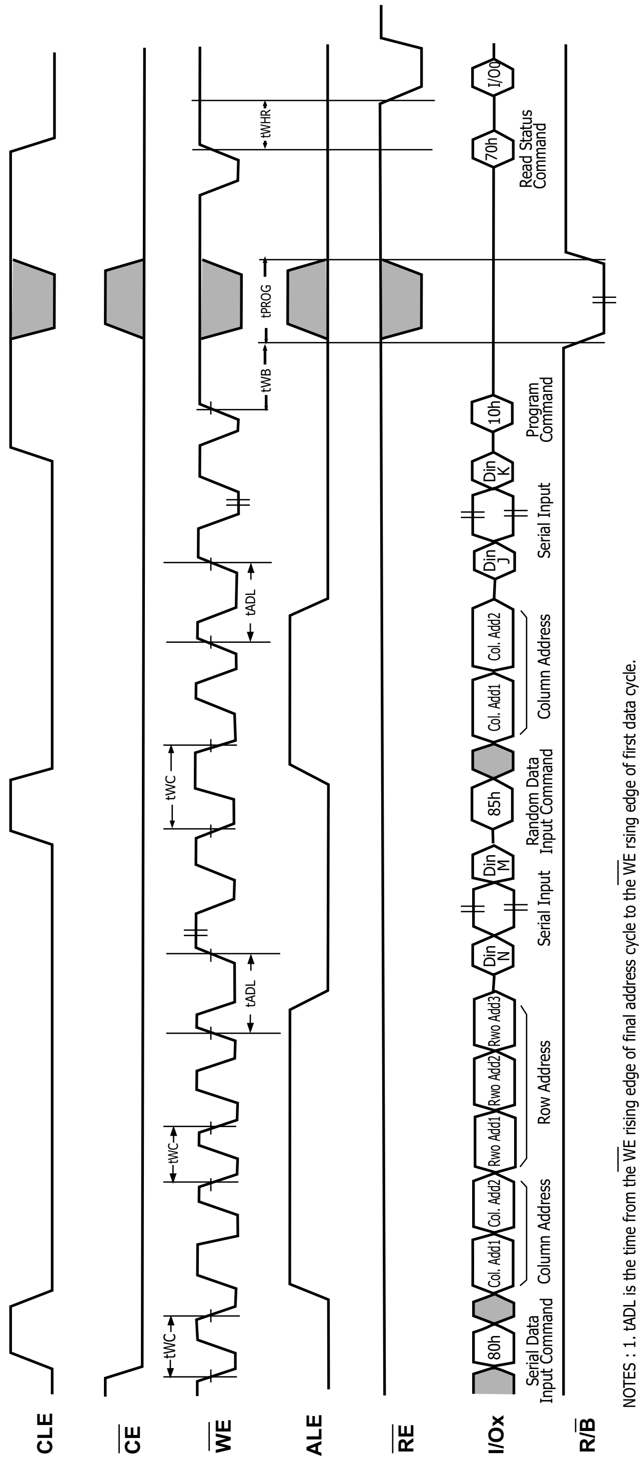


Figure 15 : Random Data In

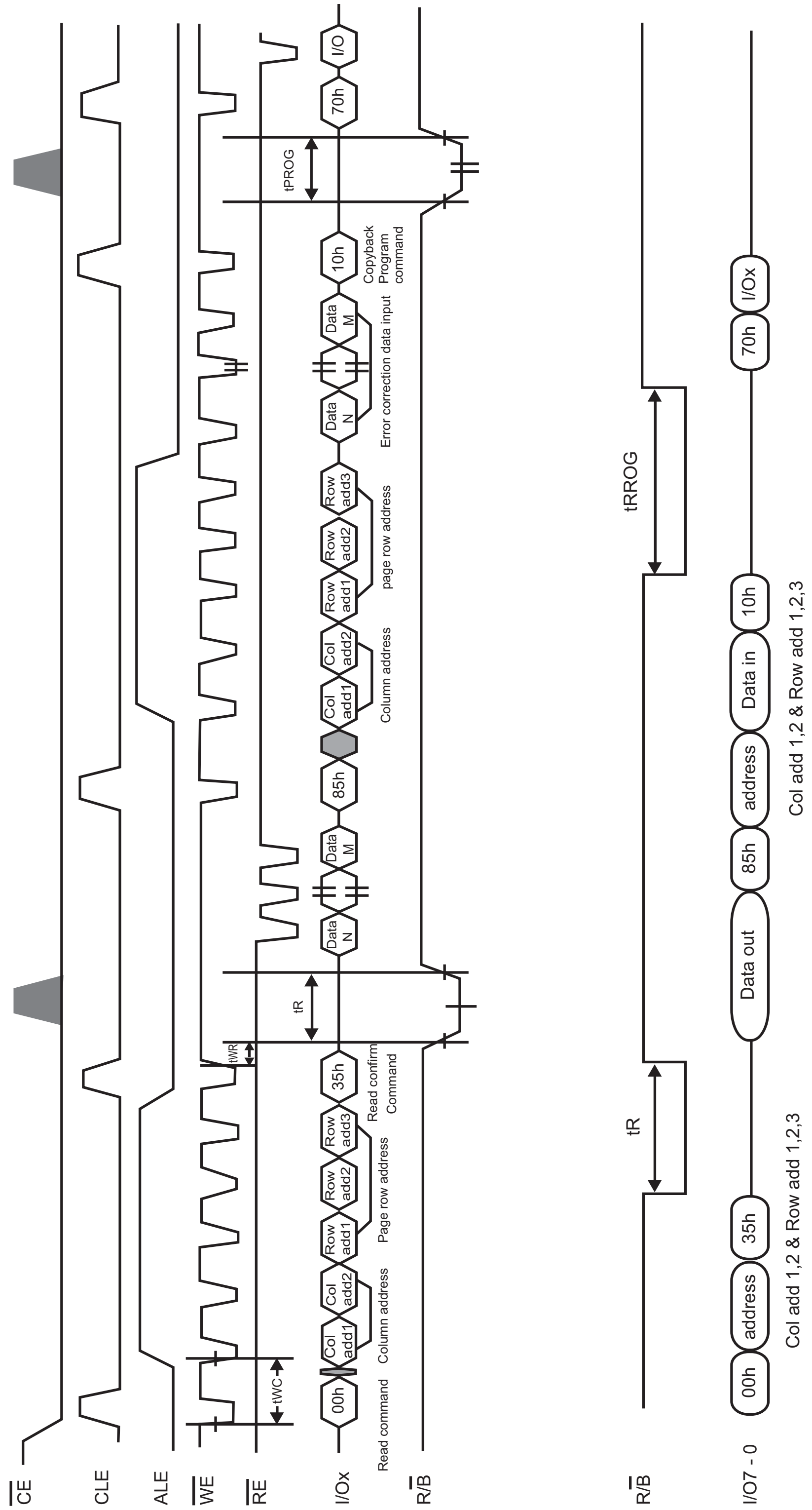


Figure 16 : Copy Back Program Operation

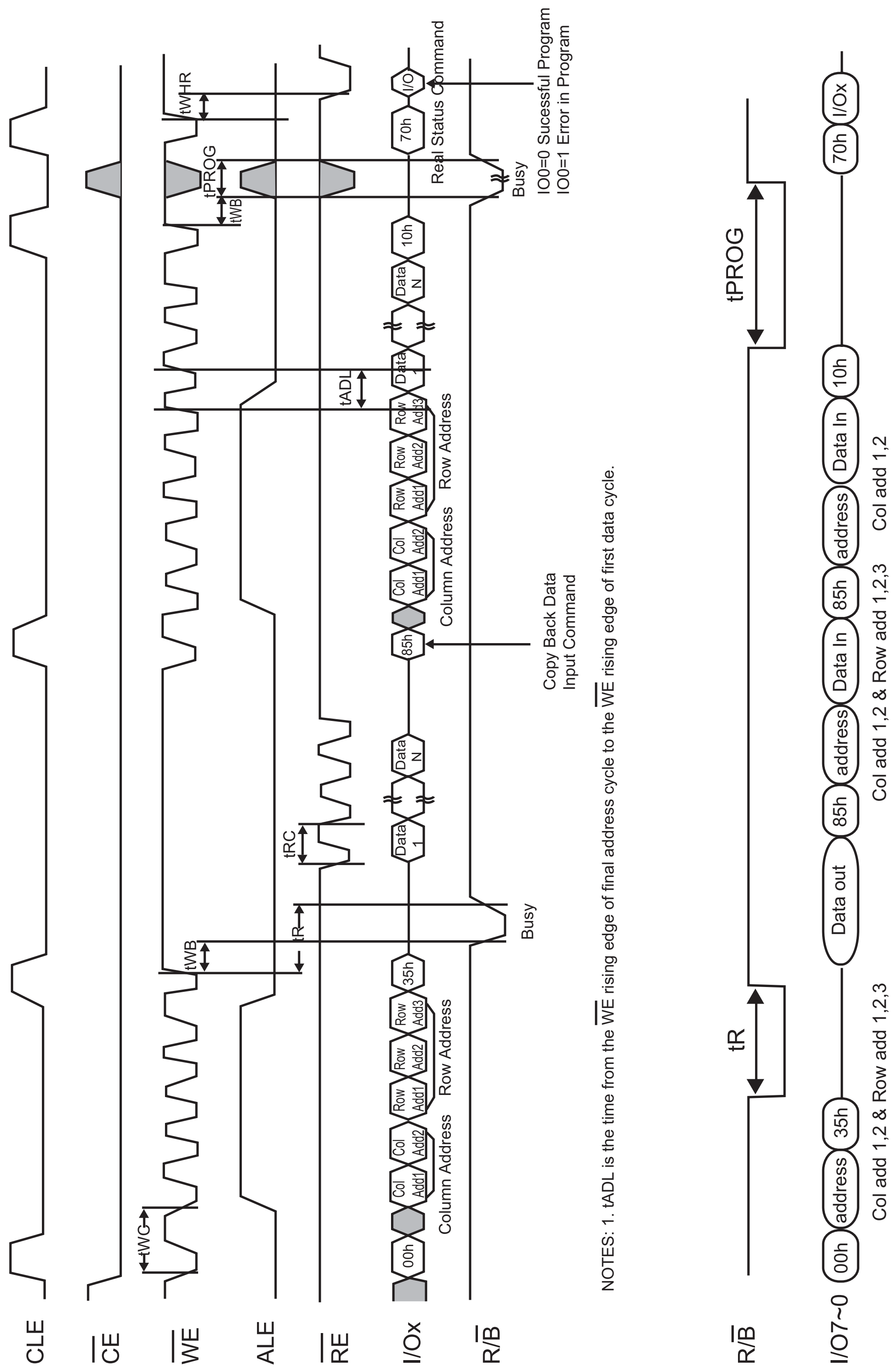


Figure 17 : Copy Back Program Operation with Random Data Input

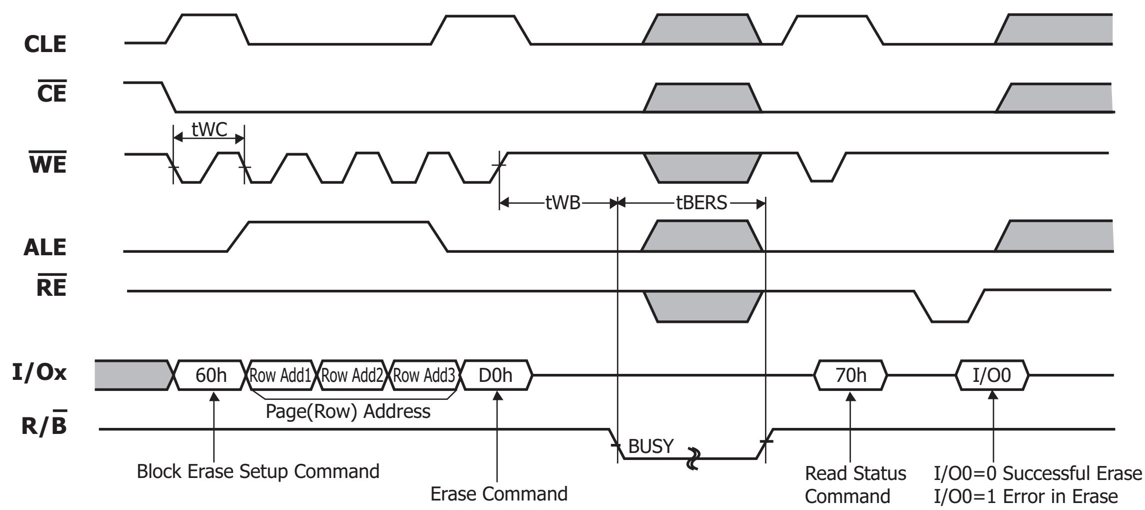


Figure 18: Block Erase Operation (Erase One Block)

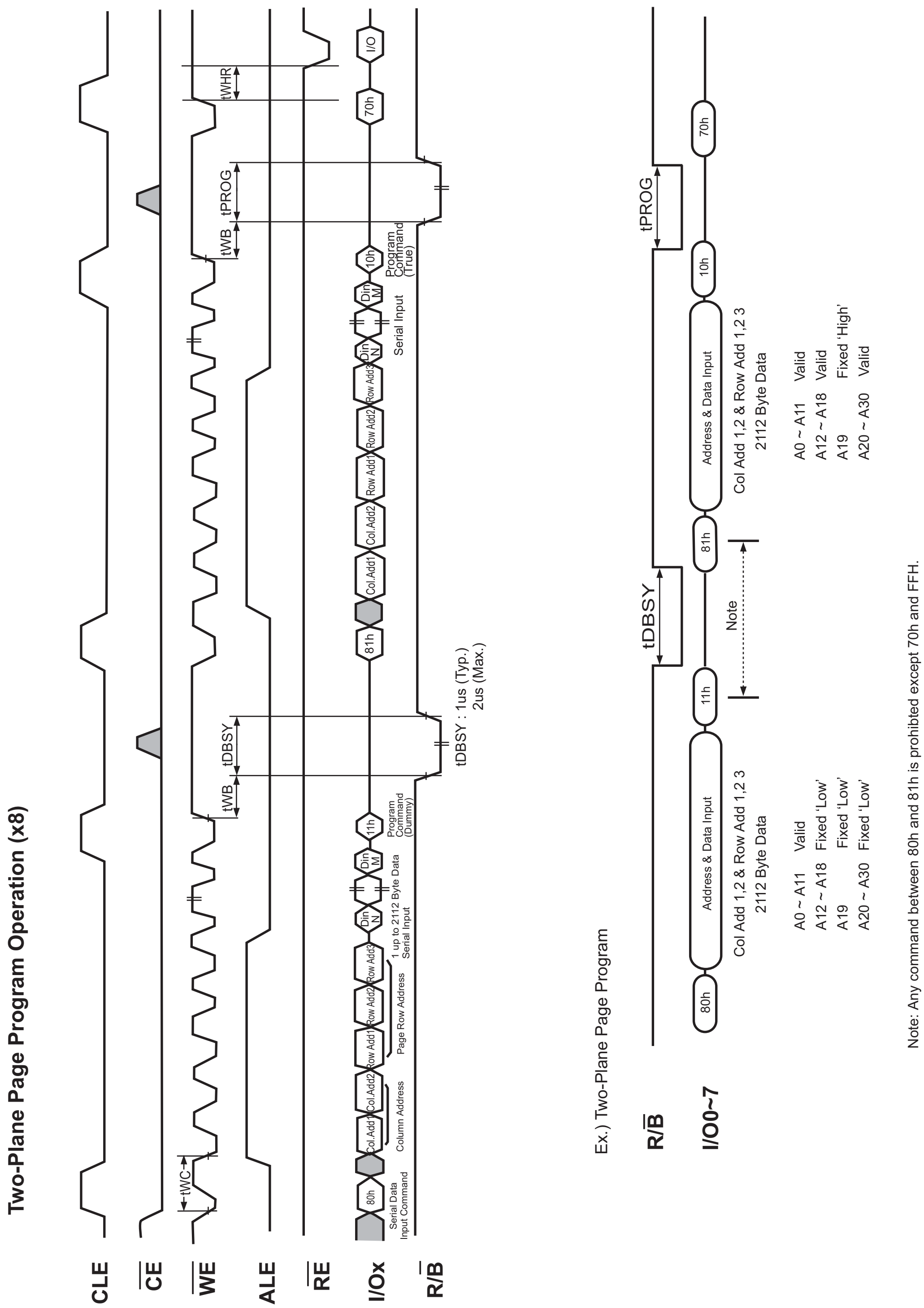
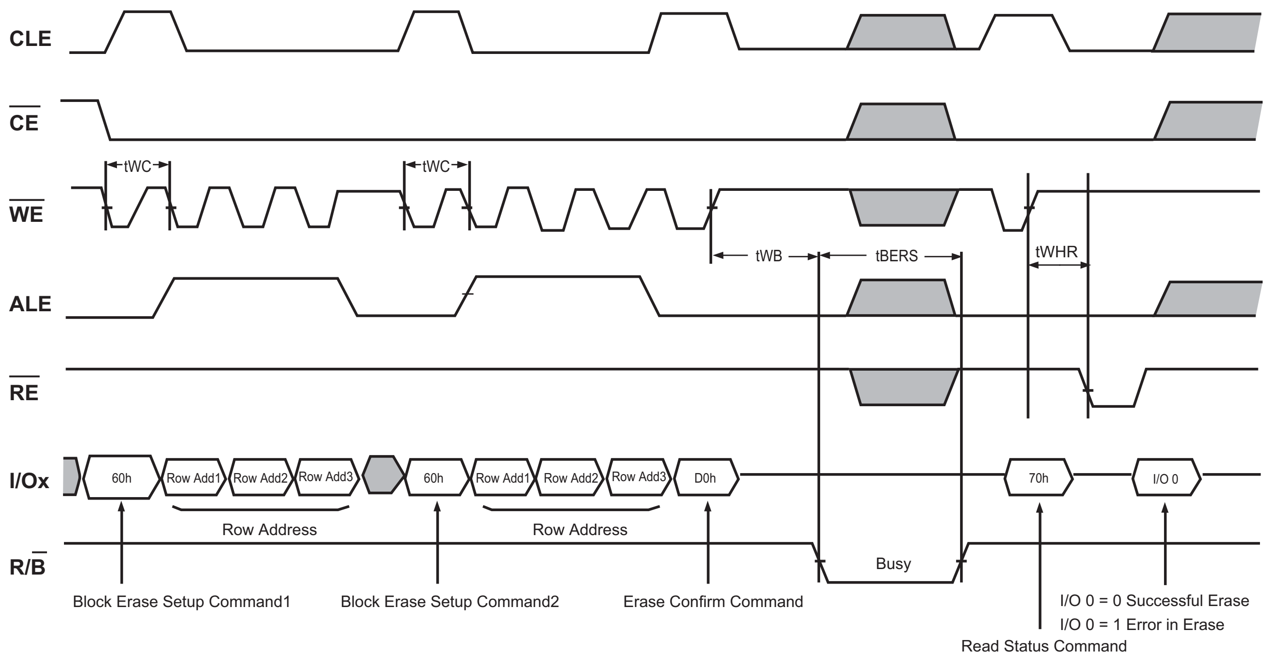


Figure 19 : Multiple plane page program



Ex.) Address Restriction for Two-Plane Block Erase Operation

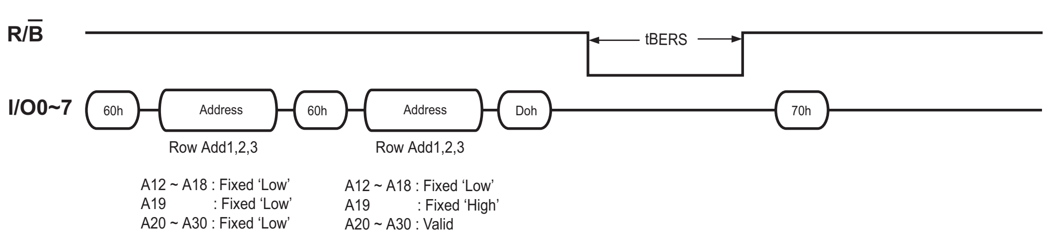


Figure 20 : Multiple plane erase operation

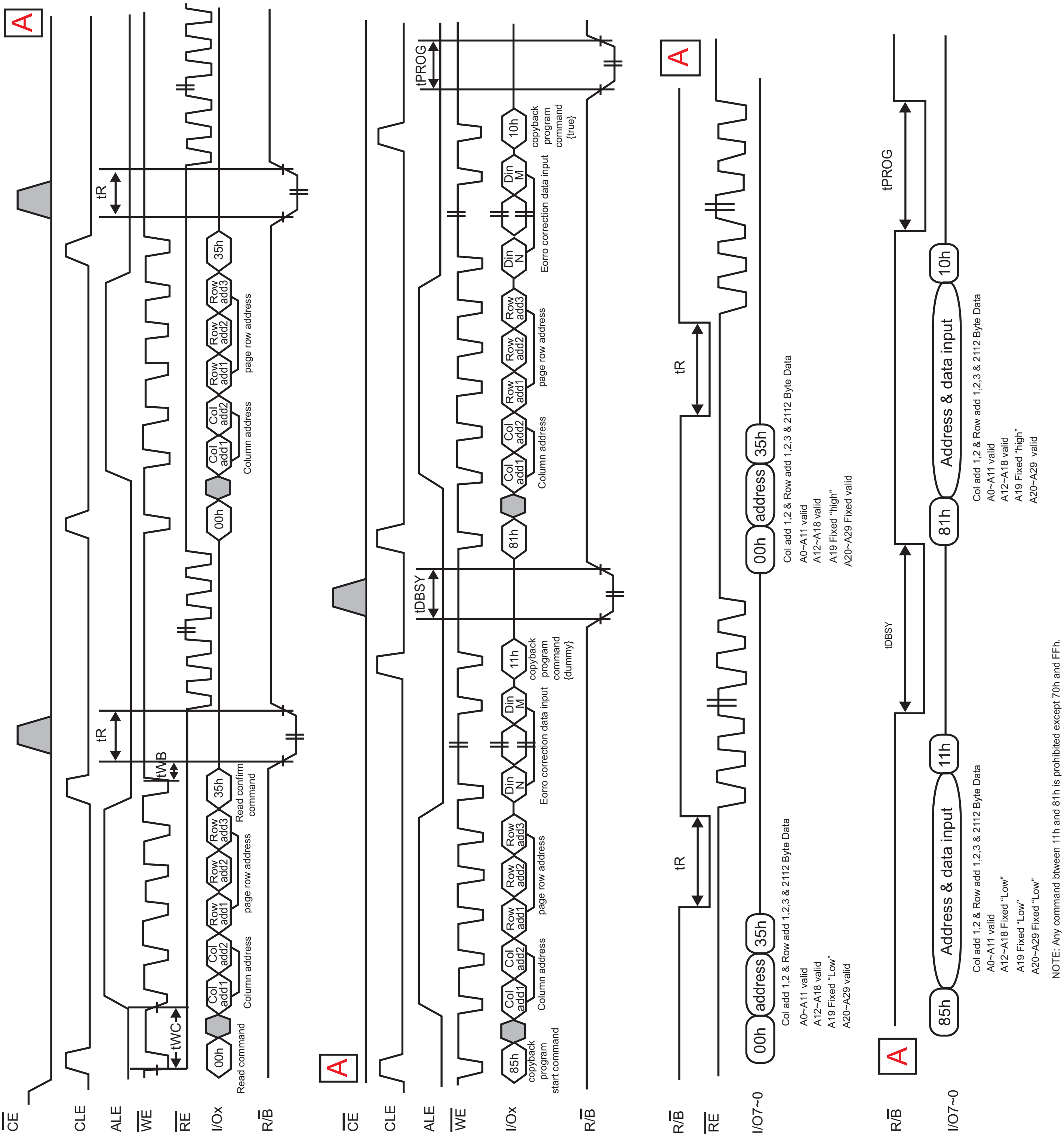


Figure 21 : Multi plane copyback program Operation

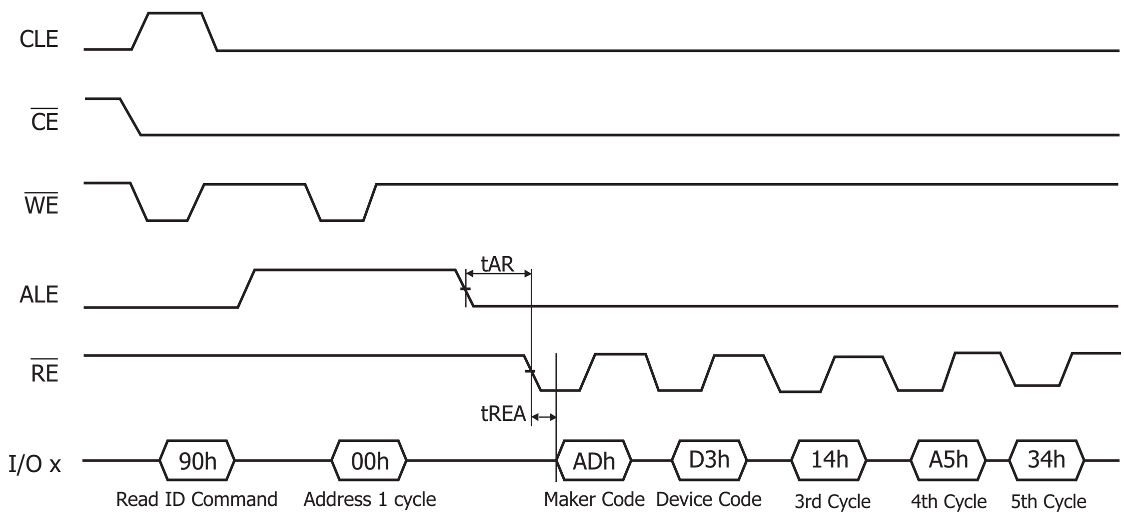


Figure 22: Read ID Operation

System Interface Using $\overline{CE}$ don't care

To simplify system interface, $\overline{CE}$ may be deasserted during data loading or sequential data-reading as shown below. So, it is possible to connect NAND Flash to a microporcessor. The only function that was removed from standard NAND Flash to make $\overline{CE}$ don't care read operation was disabling of the automatic sequential read function.

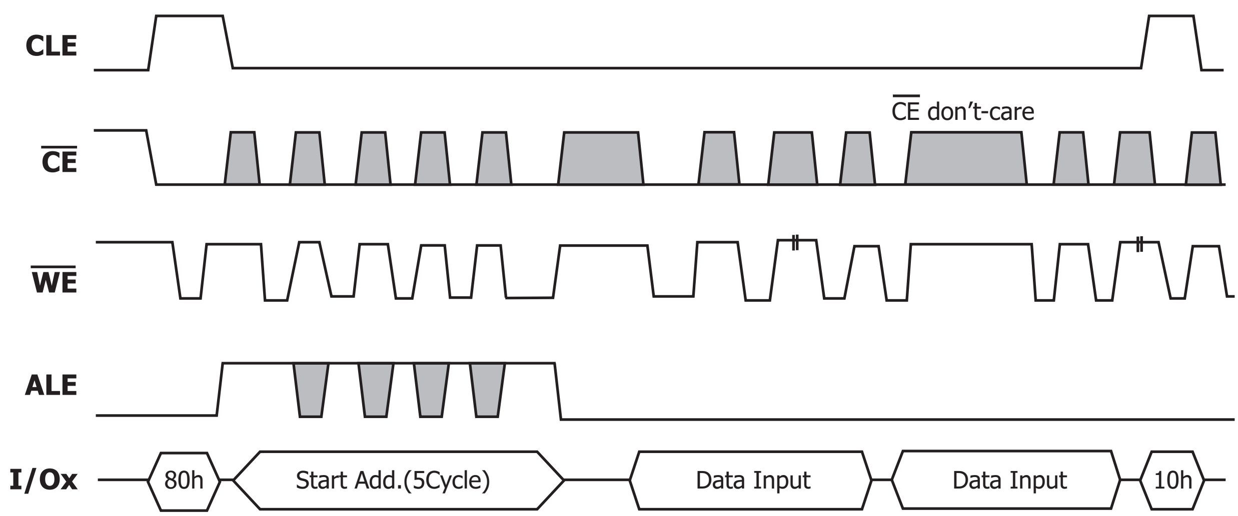


Figure 23: Program Operation with $\overline{CE}$ don't-care.

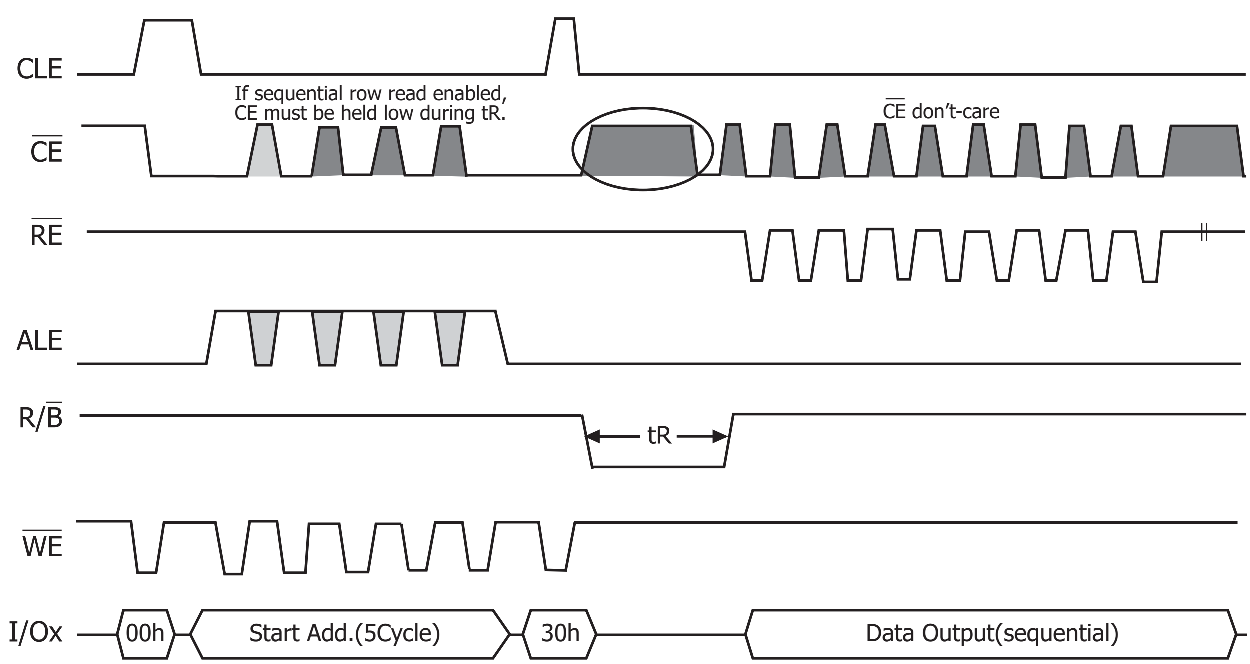


Figure 24: Read Operation with $\overline{CE}$ don't-care.

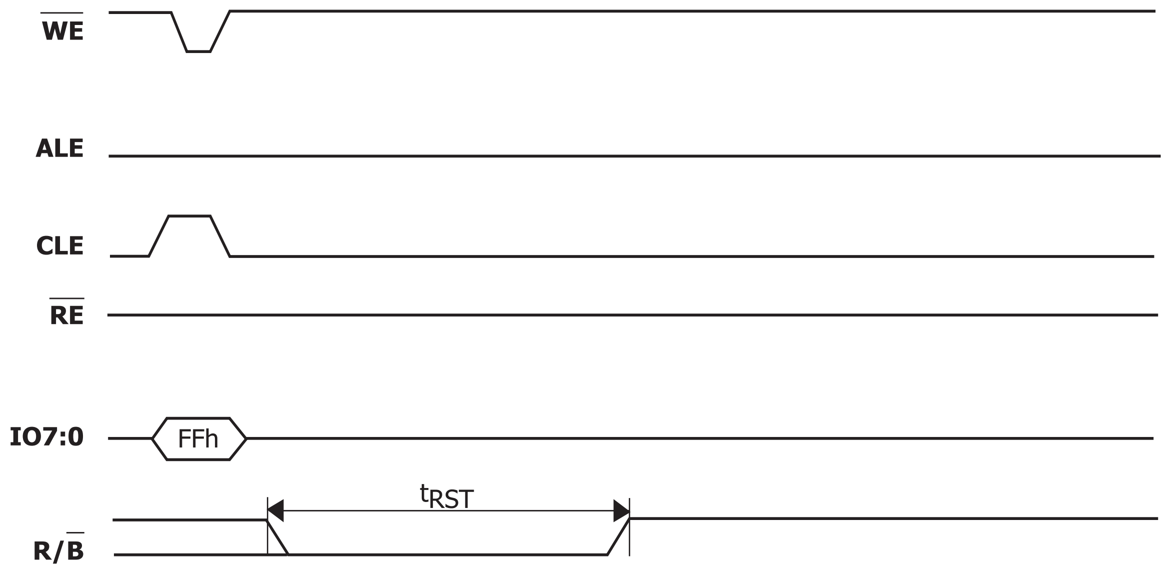


Figure 25: Reset Operation

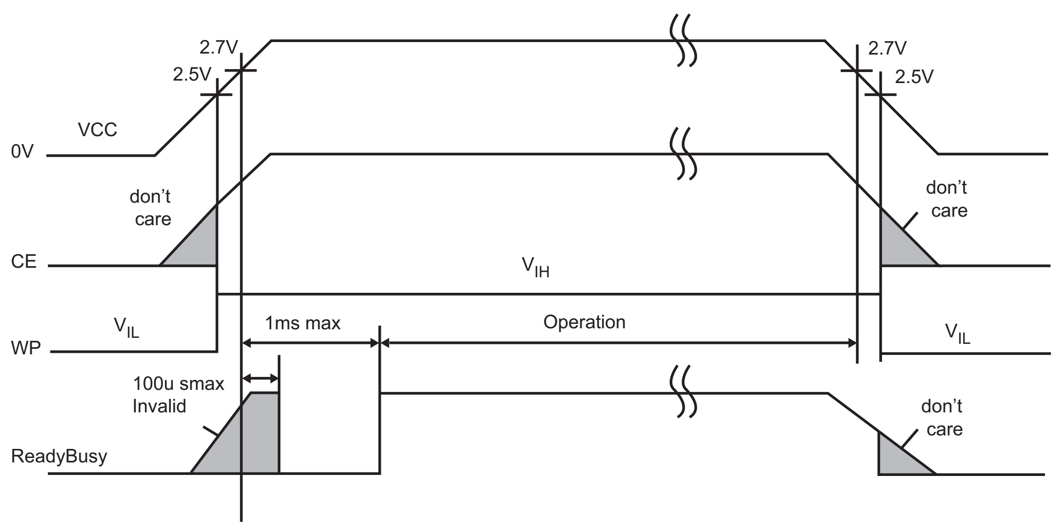


Figure 26: Power On and Data Protection Timing

VTH = 2.5 Volt for 3.3 Volt Supply devices

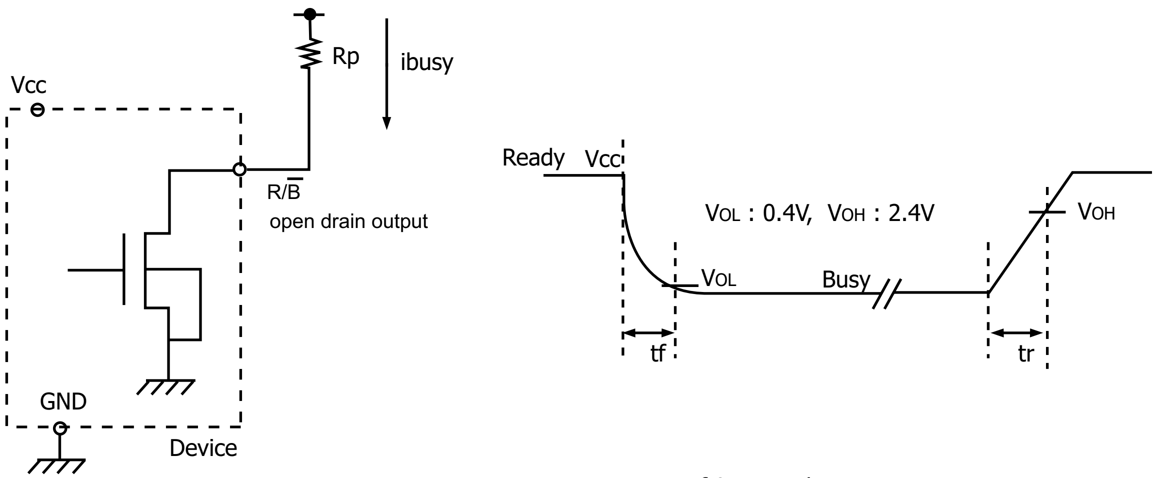
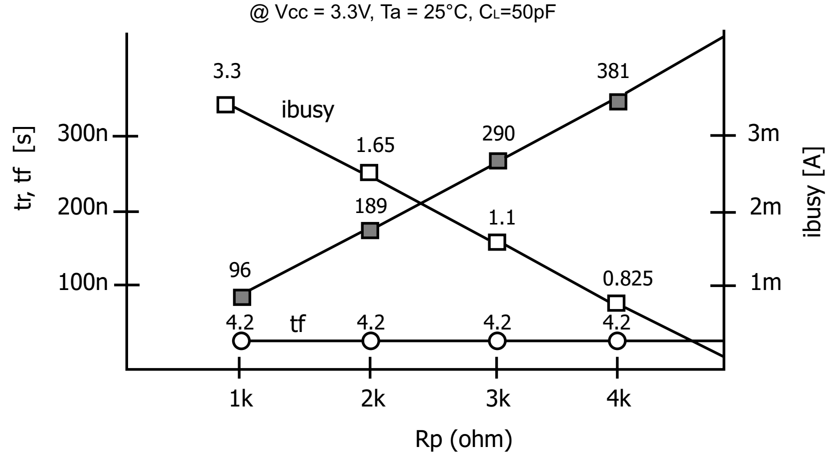


Fig. Rp vs tr, tf & Rp vs ibusy

@ Vcc = 3.3V, Ta = 25°C, CL=50pF



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{3.2V}{8mA + \sum I_L}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 27: Ready/Busy Pin electrical specifications

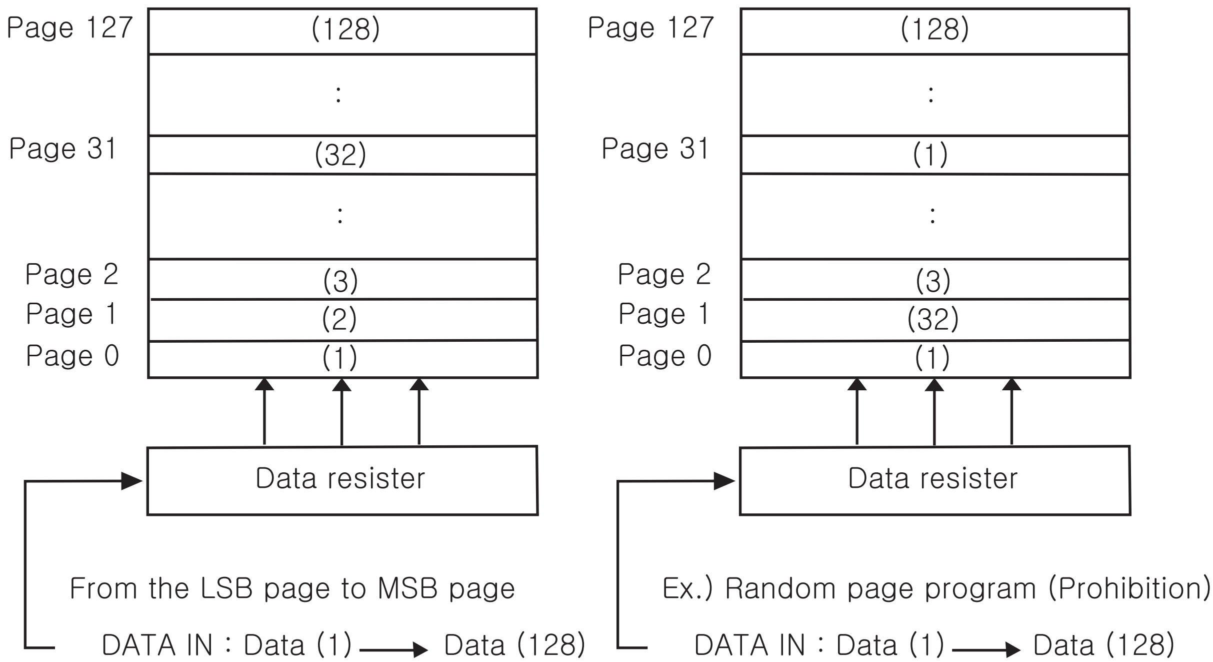


Figure 28: page programming within a block

Bad Block Management

Devices with Bad Blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A Bad Block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor. The devices are supplied with all the locations inside valid blocks erased(FFh). The Bad Block Information is written prior to shipping. Any block where the 1st Byte in the spare area of the Last or (Last-2)th page (if the last page is Bad) does not contain FFh is a Bad Block. The Bad Block Information must be read before any erase is attempted as the Bad Block Information may be erased. For the system to be able to recognize the Bad Blocks based on the original information it is recommended to create a Bad Block table following the flowchart shown in Figure 29. The 1st block, which is placed on 00h block address is guaranteed to be a valid block.

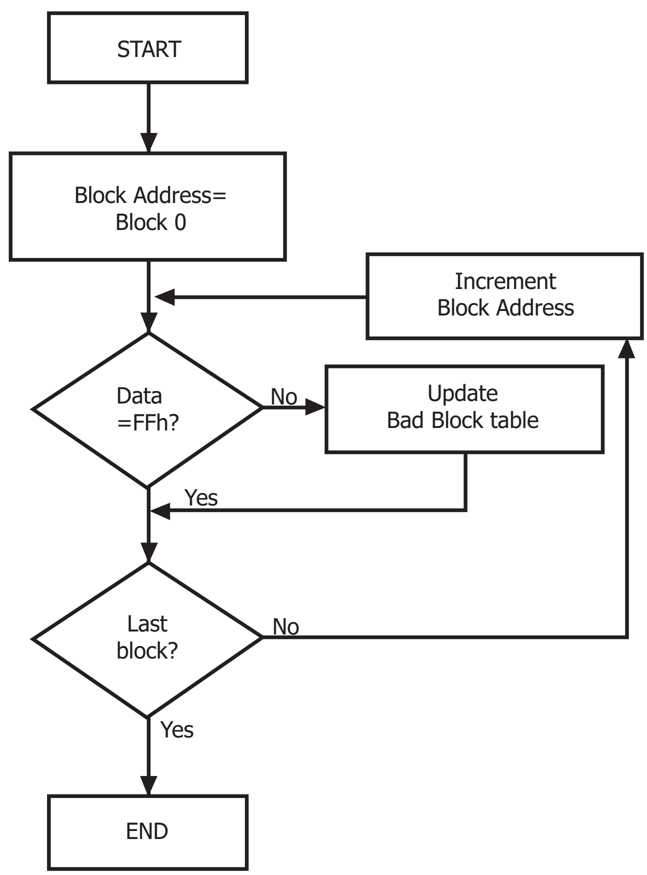


Figure 29: Bad Block Management Flowchart

NOTE :

1. Make sure that FFh at the column address 2048 of the last page and last - 2^{th} page.

Bad Block Replacement

Over the lifetime of the device additional Bad Blocks may develop. In this case the block has to be replaced by copying the data to a valid block. These additional Bad Blocks can be identified as attempts to program or erase them will give errors in the Status Register.
Unlike the case of odd page which carries a possibility of affecting previous page, the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.
Refer to Table 20 and Figure 30 for the recommended procedure to follow if an error occurs during an operation.

Operation	Recommended Procedure
Erase	Block Replacement
Program	Block Replacement
Read	ECC (with 4bit/528byte)

Table 20: Block Failure

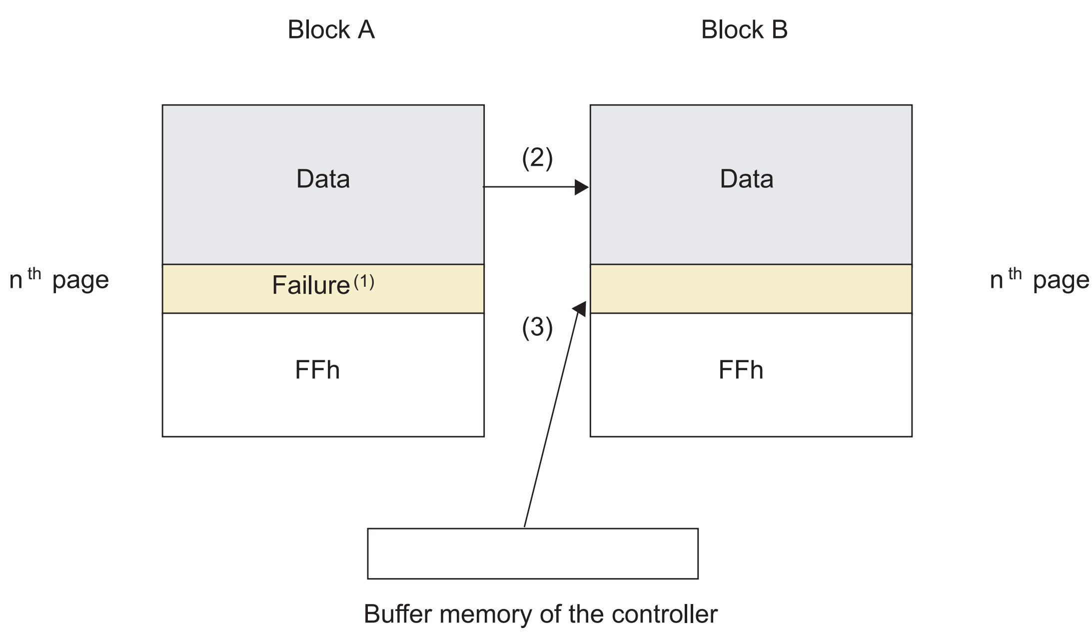


Figure 30: Bad Block Replacement

NOTE :
1. An error occurs on nth page of the Block A during program or erase operation.
2. Data in Block A is copied to same location in Block B which is valid block.
3. Nth data of block A which is in controller buffer memory is copied into nth page of Block B
4. Bad block table should be updated to prevent from eraseing or programming Block A

Write Protect Operation

The Erase and Program Operations are automatically reset when $\overline{WP}$ goes Low (tWW = 100ns, min). The operations are enabled and disabled as follows (Figure 31~34)

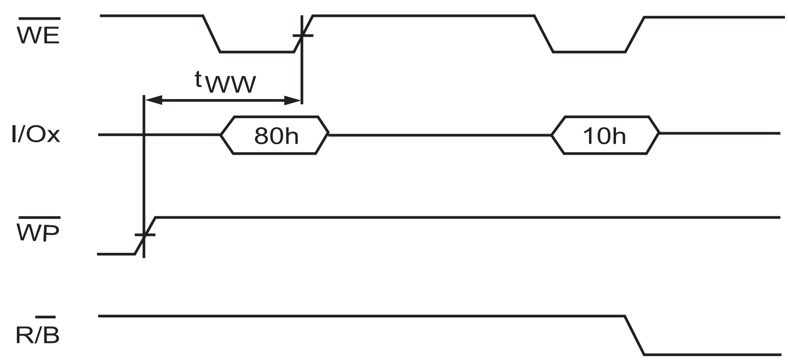


Figure 31: Enable Programming

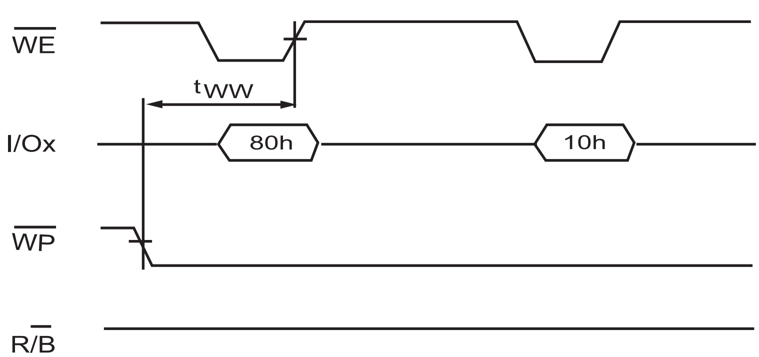


Figure 32: Disable Programming

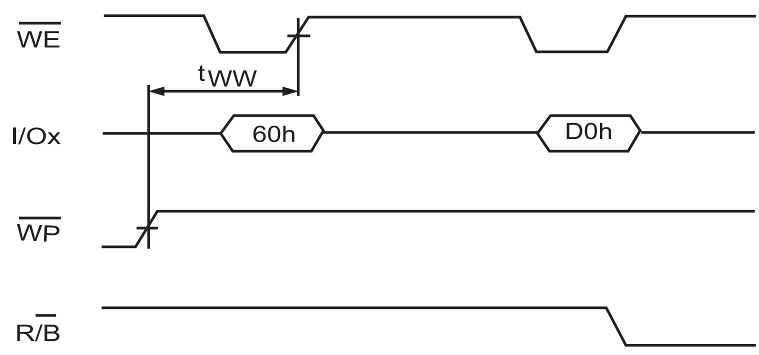


Figure 33: Enable Erasing

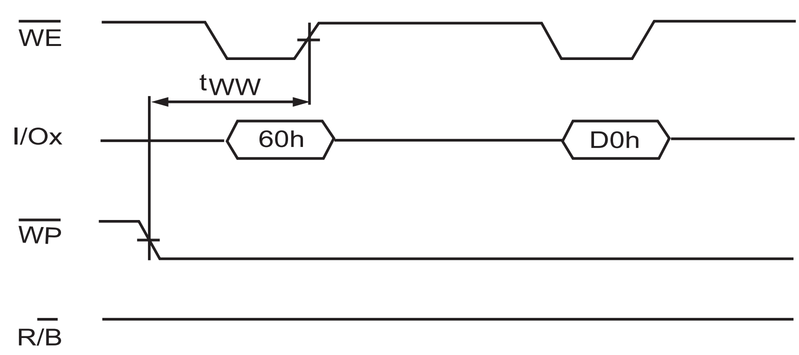


Figure 34: Disable Erasing

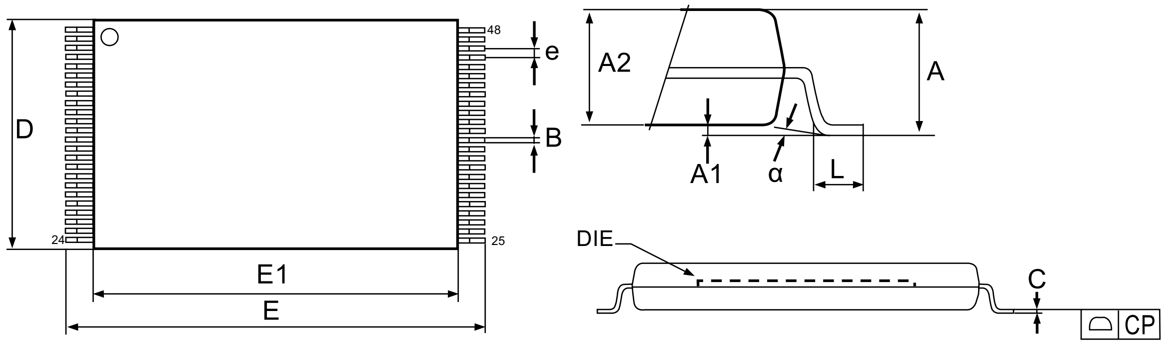


Figure 35. 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Outline

Symbol	millimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 21: 48-TSOP1 - 48-lead Plastic Thin Small Outline, 12 x 20mm, Package Mechanical Data

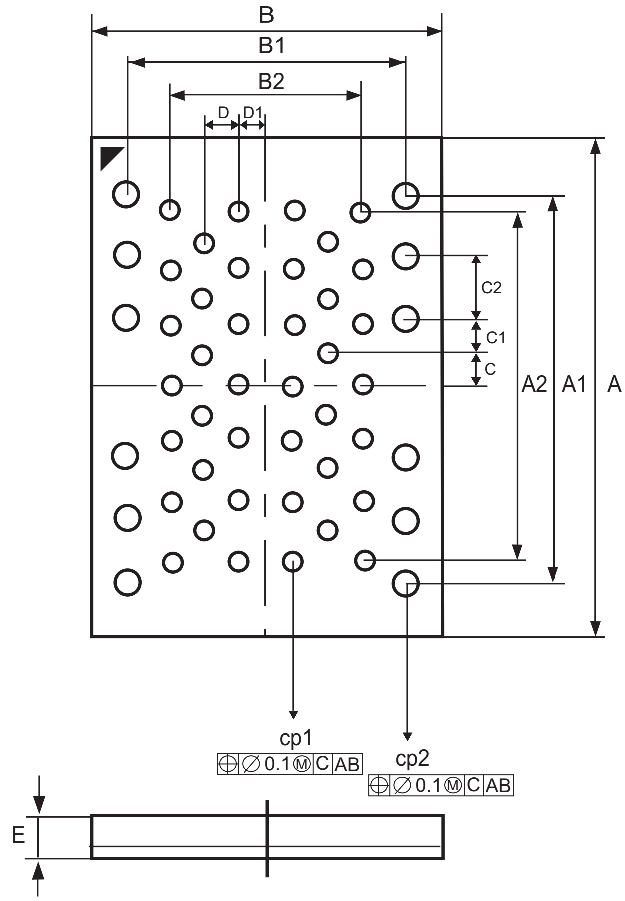


Figure 36. 52-ULGA, 12 x 17mm, Package Outline
(Top view through package)

Symbol	millimeters		
	Min	Typ	Max
A	16.90	17.00	17.10
A1		13.00	
A2		12.00	
B	11.90	12.00	12.10
B1		10.00	
B2		6.00	
C		1.00	
C1		1.50	
C2		2.00	
D		1.00	
D1		1.00	
E	0.55	0.60	0.65
CP1	0.65	0.70	0.75
CP2	0.95	1.00	1.05

Table 22: 52-ULGA, 12 x 17mm, Package Mechanical Data

Paired Page Address Information

Paired Page Address		Paired Page Address	
00h	04h	01h	05h
02h	08h	03h	09h
06h	0Ch	07h	0Dh
0Ah	10h	0Bh	11h
0Eh	14h	0Fh	15h
12h	18h	13h	19h
16h	1Ch	17h	1Dh
1Ah	20h	1Bh	21h
1Eh	24h	1Fh	25h
22h	28h	23h	29h
26h	2Ch	27h	2Dh
2Ah	30h	2Bh	31h
2Eh	34h	2Fh	35h
32h	38h	33h	39h
36h	3Ch	37h	3Dh
3Ah	40h	3Bh	41h
3Eh	44h	3Fh	45h
42h	48h	43h	49h
46h	4Ch	47h	4Dh
4Ah	50h	4Bh	51h
4Eh	54h	4Fh	55h
52h	58h	53h	59h
56h	5Ch	57h	5Dh
5Ah	60h	5Bh	61h
5Eh	64h	5Fh	65h
62h	68h	63h	69h
66h	6Ch	67h	6Dh
6Ah	70h	6Bh	71h
6Eh	74h	6Fh	75h
72h	78h	73h	79h
76h	7Ch	77h	7Dh
7Ah	7Eh	7Bh	7Fh

Note: When program operation is abnormally aborted (ex. power-down, reset), not only page data under program but also paired page data may be damaged.

Table 23: Paired Page Address Information

MARKING INFORMATION - TSOP1 / ULGA

Packag	Marking Example
TSOP1 / ULGA	hynix K O R H Y 2 7 U U 0 8 A G x A x x x x Y W W x x

- hynix	: Hynix Symbol
- KOR	: Origin Country
- HY27UU08AGxA xxxx	: Part Number
HY: Hynix	
27: NAND Flash	
U: Power Supply	: U(2.7V~3.6V)
U: Classification	: Multi Level Cell+Double Die+Large Block
08 : Bit Organization	: 08(x8)
AG: Density	: 16Gbit
x: Mode	: 5(2nCE & 2R/nB; Sequential Row Read Disable) D(Dual Interface; Sequential Row Read Disable)
A: Version	: 2nd Generation
x: Package Type	: T(48-TSOP1), U(52-ULGA)
x: Package Material	: Blank(Normal), P(Lead Free)
x: Operating Temperature	: C(0℃~70℃), I(-40℃~85℃)
x: Bad Block	: B(Included Bad Block), S(1~5 Bad Block), P(All Good Block)
- Y: Year (ex: 5=year 2005, 6= year 2006)	
- ww: Work Week (ex: 12= work week 12)	
- xx: Process Code	

Note

- Capital Letter	: Fixed Item
- Small Letter	: Non-fixed Item