Document Title

2Bank x 512K x 16bits Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	Feb. 2006	Preliminary
0.2	Final Revision	Apr. 2006	

DESCRIPTION

THE Hynix HY57V161610F-Series is a 16,777,216-bits CMOS Synchronous DRAM, ideally suited for the main memory and graphic applications which require large memory density and high bandwidth. HY57V161610F-Series is organized as 2banks of 524,288x16.

HY57V161610F-Series is offering fully synchronous operation referenced to a positive edge clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 1,2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipeline design is not restricted by a '2N' rule.)

FEATURES

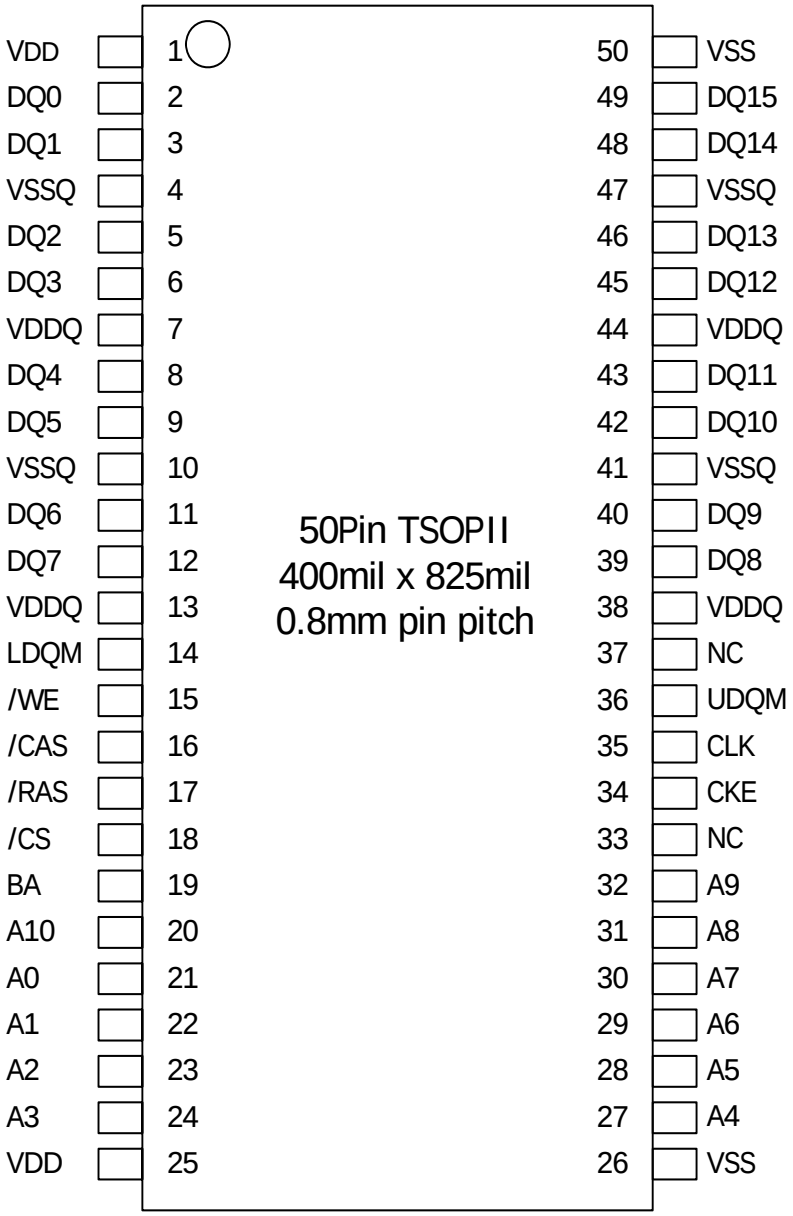
- Voltage: VDD, VDDQ 3.3V supply voltage
- All device pins are compatible with LVTTL interface
- JEDEC standard 400mil 50pin TSOP-II with 0.8mm of pin pitch (Lead or Lead Free Package)
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by UDQM, LDQM
- Internal two banks operation
- Auto refresh and self refresh
- 4096 Refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency; 1, 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION (VDD(min) of HY57V161610FT(P)-5(I) series is 3.15V)

Part No.	Clock Frequency	Organization	Interface	Package
HY57V161610FT(P)-5(I)	200MHz	2Banks x 512Kbits x16I/O	LVTTL	400mil 50TSOPII
HY57V161610FT(P)-6(I)	166MHz			
HY57V161610FT(P)-7(I)	143MHz			
HY57V161610FT(P)-H(I)	133MHz			

Note: 1. HY57V161610FTP Series: Lead free, commercial temperature(0°C ~ 70°C.)
2. HY57V161610FT Series: Leaded, commercial temperature(0°C ~ 70°C.)
3.HY57V161610FTP-xxI Series: Lead free, Industrial temperature(-40°C ~ 85°C)
4.HY57V161610FT-xxI Series: Leaded, Industrial temperature(-40°C ~ 85°C)

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
CLK	INPUT	Clock: The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	INPUT	Clock Enable: Controls internal clock signal and when deactivated, the SDRAM will be one of the states among (deep) power down, suspend or self refresh
$\overline{CS}$	INPUT	Chip Select: Enables or disables all inputs except CLK, CKE, and DQM
BA	INPUT	Bank Address: Select either one of banks during both $\overline{RAS}$ and $\overline{CAS}$ activity
A0 ~ A10	INPUT	Row Address: RA0 ~ RA10, Column Address: CA0 ~ CA7 Auto-precharge flag: A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	INPUT	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
UDQM, LDQM	INPUT	Data Mask: Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	I/O	Data Input / Output: Multiplexed data input / output pin
V_{DD}/V_{SS}	SUPPLY	Power supply for internal circuits
V_{DDQ}/V_{SSQ}	SUPPLY	Power supply for output buffers
NC	-	No connection : These pads should be left unconnected

FUNCTIONAL BLOCK DIAGRAM

512K x 2Banks x 16 I/O Synchronous DRAM