Samsung e·MMC Product family

e.MMC 4.41 Specification compatibility

datasheet

Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	1. Customer Sample	May. 19, 2014	Final	S.M.Lee

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INTRODUCTION

The SAMSUNG e·MMC is an embedded MMC solution designed in a BGA package form. e·MMC operation is identical to a MMC card and therefore is a simple read and write to memory using MMC protocol v4.41 which is a industry standard.

e·MMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF) whereas 1.8V or 3V dual supply voltage (VDD) is supported for the MMC controller. Maximum MMC interface frequency of 52MHz and maximum bus widths of 8 bit are supported.

There are several advantages of using e·MMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market.

The embedded flash mangement software or FTL(Flash Transition Layer) of e·MMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

1.0 PRODUCT LIST

[Table 1] Product List

Capacities	e·MMC Part ID	NAND Flash Type	User Density (%)	Power System	Package size	Pin Configuration
4 GB	KLM4G1YE4C-B0020YB	32Gb TLC x 1	92.19%	- Interface power : VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) - Memory power : VDDF (2.7V ~ 3.6V)	11.5mm x 13mm x 1.0mm	153FBGA

2.0 KEY FEATURES

• embedded MultiMediaCard System Specification Ver. 4.41 compatible. Detail description is referenced by JEDEC Standard

• SAMSUNG e·MMC supports below special features which are defined in JEDEC

- High Priority Interrupt scheme is supported

- Background operation is supported.

• Full backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-e·MMC systems)

• Data bus sidth :1bit(Default), 4bit and 8bit

• MMC I/F Clock Frequency : 0 ~ 52MHz
MMC I/F Boot Frequency : 0 ~ 52MHz

• Dual Data Rate mode is supported

• Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)

• Power : Interface power → VDD (1.70V ~ 1.95V or 2.7V ~ 3.6V) , Memory power → VDDF(2.7V ~ 3.6V)

3.0 PACKAGE CONFIGURATIONS

3.1 153 Ball Pin Configuration

[Table 2] 153 Ball Information

Pin NO	Name
A3	DAT0
A4	DAT1
A5	DAT2
B2	DAT3
B3	DAT4
B4	DAT5
B5	DAT6
B6	DAT7
K5	RSTN
C6	VDD
M4	VDD
N4	VDD
P3	VDD
P5	VDD
E6	VDDF
F5	VDDF
J10	VDDF
K9	VDDF
C2	VDDI
M5	CMD
M6	CLK
C4	VSS
E7	VSS
G5	VSS
H10	VSS
K8	VSS
N2	VSS
N5	VSS
P4	VSS
P6	VSS

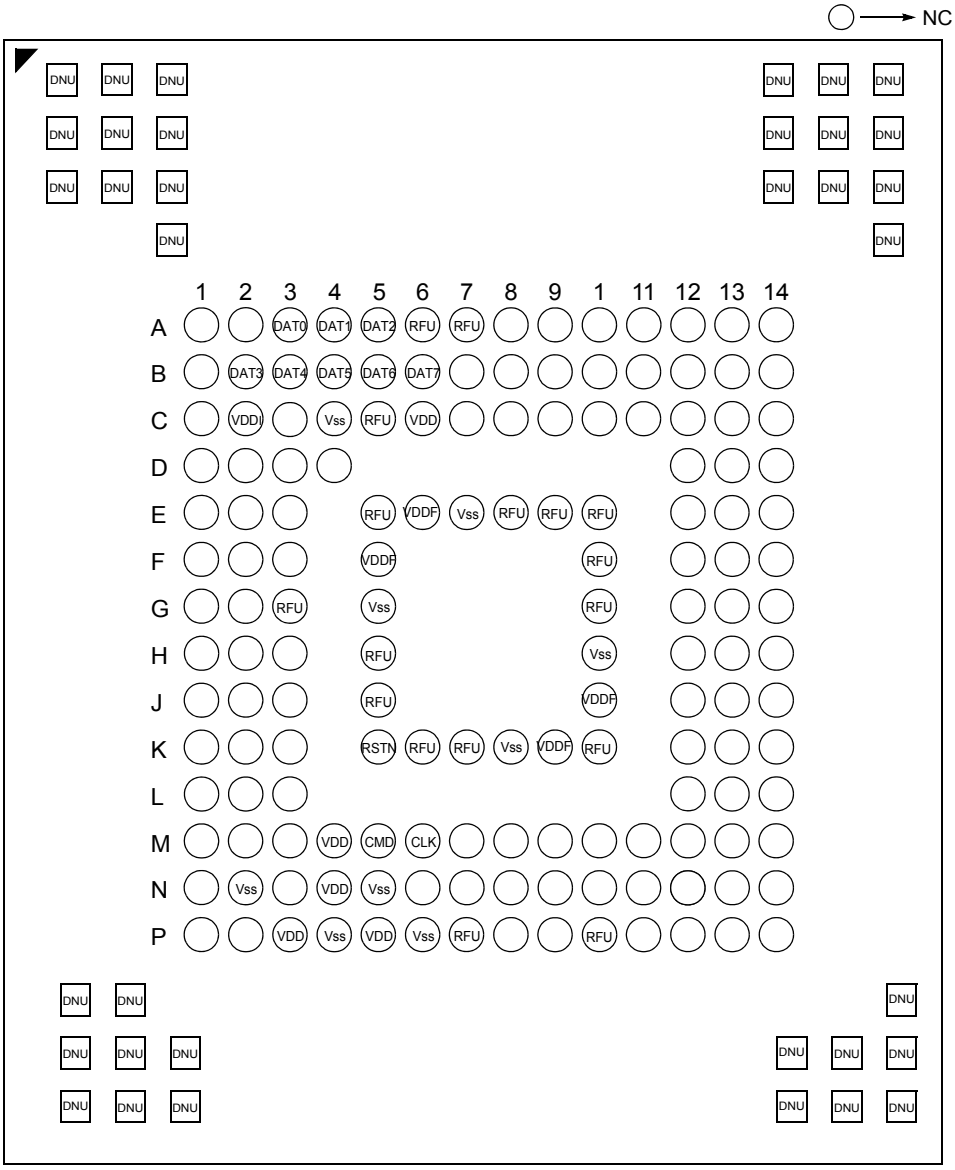


Figure 1. 153-FBGA

3.1.1 11.5mm x 13mm x 1.0mm Package Dimension

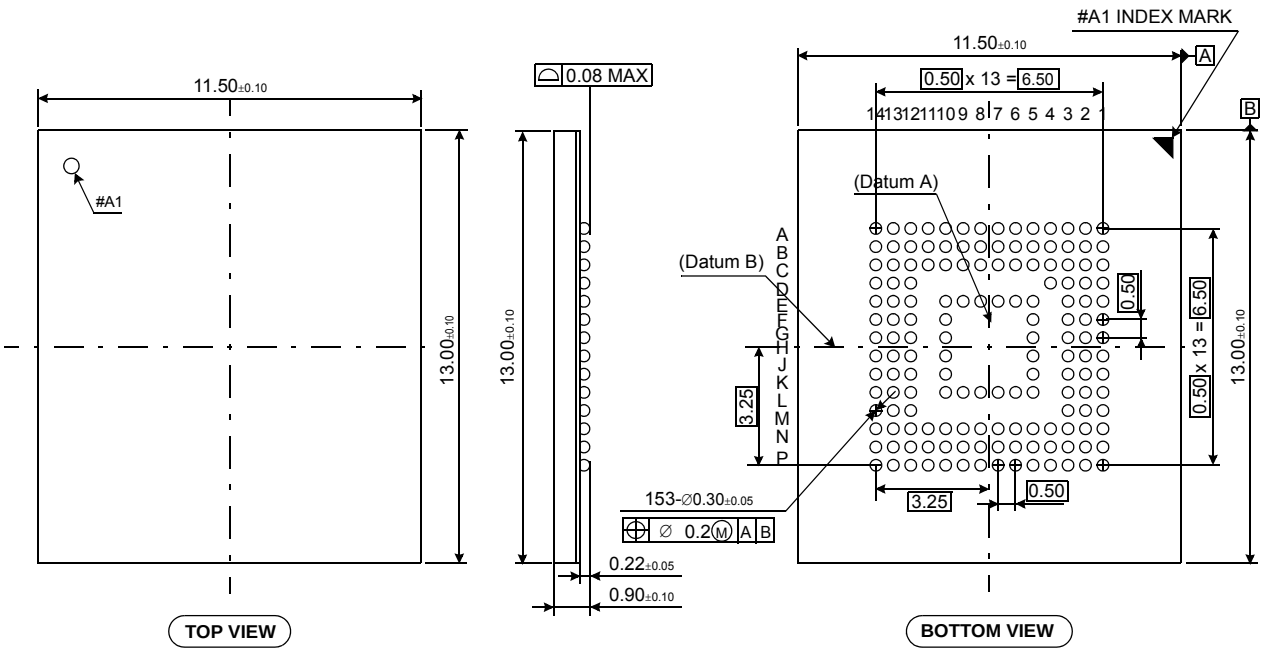


Figure 2. 11.5mm x 13mm x 1.0mm Package Dimension

3.2 Product Architecture

- e·MMC consists of NAND Flash and Controller. VDD is for Controller power and VDDF is for flash power

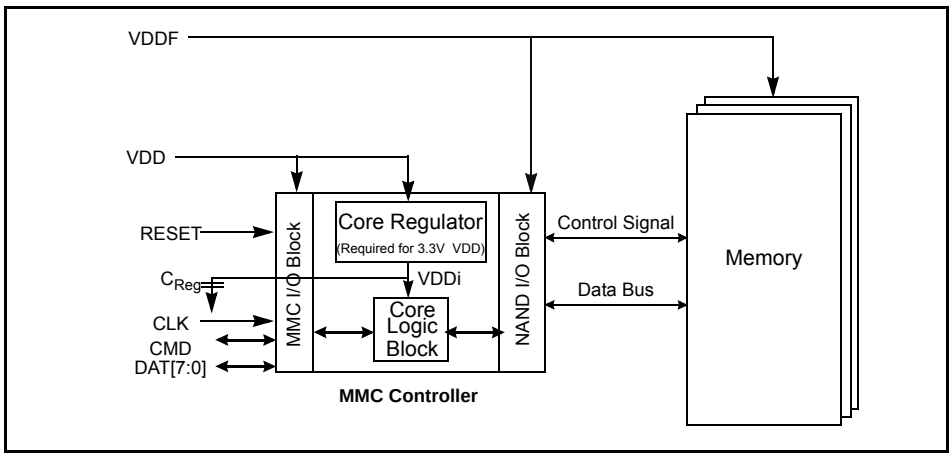


Figure 3. e·MMC Block Diagram

4.0 e.MMC 4.41 features

4.1 Data Write

Host can configure reliability mode to protect existing data per each partition.

This relibility mode has to be set before partitioning is completed.

This reliability setting only impacts the reliability of the main user area and the general purpose partitions.

[Table 3] EXT_CSD value for reliability setting in write operation

Name	Field	Size (Bytes)	Cell Type	EXT_CSD-slice	Value
Data Reliability Configuration	WR_REL_SET	1	R/W	[167]	0x1F
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Explanation of each field in the upper table is mentioned below

[Table 4] Definition of EXT_CSD value for reliability setting

Fields	Definitions
HS_CTRL_REL	0x0: All the WR_DATA_REL parameters in the WR_REL_SET registers are read only bits. 0x1: All the WR_DATA_REL parameters in the WR_REL_SET registers are R/W.
EN_REL_WR	0x0: The device supports the previous definition of reliable write. 0x1: The device supports the enhanced definition of reliable write

The below table shows each field for WE_REL_SET

[Table 5] Description of each field for WE_REL_SET

Name	Field	Bit	Size	Type
Write Data Reliability (user Area)	WR_DATA_REL_USR	0	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 1	WR_DATA_REL_1	1	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 2	WR_DATA_REL_2	2	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 3	WR_DATA_REL_3	3	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Write Data Reliability Partition 4	WR_DATA_REL_4	4	1	R (if HS_CTRL_REL=0) R/W (if HS_CTRL_REL=1)
Reserved	-	7:5	-	-

4.2 Reliable Write

[Table 6] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Data Reliability Supports	WR_REL_PARAM	1	R	[166]	0x05

Reliable write with EN_REL_WR is 0x1 supports atomicity of sector unit.

The block size defined by SET_BLOCKLEN (CMD16) is ignored and reliable write is executed as only 512 byte length. There is no limit on the size of the reliable write.

[Table 7] EXT_CSD value for reliable write

Name	Field	Size (Bytes)	Cell Type	CSD-slice	Value
Reliable Write Sector Count	REL_WR_SEC_C	1	R	[222]	0x01

4.3 Secure Trim

Secure Trim operation consists of Secure Trim Step1 and Secure Trim Step2.
In Secure Trim Step 1 the host defines the range of write blocks that it would like to mark for the secure purge.

[Table 8] EXT_CSD value for secure trim

Field	Definitions	Value
SEC_TRIM_MULT	Secure Trim Step2 Timeout = 300ms x ERASE_TIMEOUT_MULT x SEC_TRIM_MULT	0x11

Area marked by Secure Trim Step1 is shown as EXT_CSD[181](ERASED_MEM_CONT) before Secure Trim Step2 is completed.

When Secure Trim Step2 is issued, if there is no data marked by Secure Trim Step1, Secure Trim Step2 does not work.

4.4 High Priority Interrupt

High Priority Interrupt is to stop ongoing operation and perform read operation with high priority

Command set for High Priority Interrupt operation is the below

[Table 9] Command List for High Priority Interrupt

CMD Index	Type	Argument	Resp	Abbreviation	Command Description
CMD12	ac	[31:16] – RCA* [15:1] – stuff bits [0] – High Priority Interrupt * *To be used only to send a High Priority Interrupt	R1b	STOP_TRANSMISSION	If High Priority Interrupt flag is set the device shall interrupt its internal operations in a well defined timing

Interruptible commands by read while write operation are the below.

[Table 10] List of Interruptible Command

Commands	Names	Notes
CMD24	WRITE SINGLE BLOCK	-
CMD25	WRITE MULTIPLE BLOCKS	-
CMD25	RELIABLE WRITE	Stopping a reliable write command with 'High Priority Interrupt' flag set turns that command into a reliable write command
CMD38	ERASE	-
	TRIM	-
	SECURE ERASE	-
	SECURE TRIM	-
CMD6	SWITCH	BACKGROUND OPERATION ONLY

[Table 11] EXT_CSD value for HPI

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
HPI features	HPI_FEATURES	1	R	[503]	0x03
Number of correctiy programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	[245:242]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out of interrupt busytiming	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x02
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00

[Table 12] Definition of EXT_CSD value for HPI

Fields	Definitions
HPI_FEATURES	Bit 0 means HPI_SUPPORT Bit 0 = 0x0 : High Priority Interrupt mechanism not supported Bit 0 = 0x1 : High Priority Interrupt mechanism supported Bit 1 means HPI_IMPLEMENTATION 0x0 : HPI mechanism implementation based on CMD13 0x1 : HPI mechanism implementation based on CMD12
CORRECTLY_PRG_SECTOR_NUM	This field indicates how many 512B sectors were successfully programmed by the last WRITE_MULTIPLE_-BLOCK command (CMD25). CORRECTLY_PRG_SECTORS_NUM=EXT_CSD[242]*2^0+EXT_CSD[243]*2^8 +EXT_CSD[244]*2^16 + EXT_CSD[245]*2^24
PARTITION_SWITCH_TIME	This field indicates the maximum timeout for the SWITCH command (CMD6) when switching partitions by changing PARTITION_ACCESS bits in PARTITION_CONFIG field (EXT_CSD byte [179]). Time is expressed in units of 10 milliseconds
OUT_OF_INTERRUPT_TIME	This field indicates the maximum timeout to close a command interrupted by HPI - time between the end bit of CMD12 / CMD 13 to the DAT0 release by the device.
HPI_MGMT	Bit 0 means HPI_EN 0x0 : HPI mechanism not activated by the host 0x1 : HPI mechanism activated by the host

4.5 Background Operation

When the host is not being serviced, e·MMC can do internal operation by using “Background Operation” command. In this operation which takes long time to complete can be handled later when host ensure enough idle time (In Back ground operation)

Background Operation Sequence is the following

[Table 13] Background Operation Sequence

Function	Command	Description
Background Operation Check	CMD8 Or Card Status Register	If BKOPS_STATUS is not 0 or 6th bit of card status register is set, there are something to be performed by background operation
Background Operation Start	CMD6	Background operation starts by BKOPS_START is set to any value. When background operation is completed BKOPS_STATUS is set to 0 and BKOPS_START is set to 0.
Background Operation Stop	HPI	If the background operation is stopped BKOPS_START is set to 0

[Table 14] EXT_CSD value for Background Operation

Name	Field	Size(Bytes)	Cell Type	CSD-Slice	Value
Background operations Support	BKOPS_SUPPORT	1	R	[502]	0x01
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations hand shake	BKOP_EN	1	R/W	[163]	0x00

[Table 15] Definition of EXT_CSD value for Bakgrourd Operation

Fields	Definitions
BKOPS_SUPPORT	‘0’ means Background operation is not supported ‘1’ means Background operation is supported
BKOPS_ STATUS	‘0’ means No background work pending ‘1’ means pending background work existing. ‘2’ means pending background work existing & performance being impacted. ‘3’ means pending background work existing & critical
BKOPS_START	Background operation start while BKOPS_START is set to any value. ‘0’ means Background operation is enabled.
BKOPS_EN	‘0’ means host does not support background operation ‘1’ means host use background operation manually

[Table 16] Card Status Register for Background Operation

Bits	Identifier	Type	Det Mode	Value	Description	Clear Cond
6	URGENT_BKOPS	S	R	“0” = Not Urgent “1” = Urgent	If set, device needs to perform background operations urgently. Host can check EXT_CSD field BKOPS_STATUS for the detailed level (in case of BKOPS_STATUS is 2 or 3)	A

5.0 Technical Notes

5.1 S/W Agorithm

5.1.1 Partition Management

The device initially consists of two Boot Partitions and RPMB Partition and User Data Area.

The User Data Area can be divided into four General Purpose Area Partitions and User Data Area partition. Each of the General Purpose Area partitions and a section of User Data Area partition can be configured as enhanced partition.

5.1.1.1 Boot Area Partition and RPMB Area Partition

Boot Partition size & RPMB Partition Size are set by the following command sequence :

[Table 17] Setting sequence of Boot Area Partition size and RPMB Area Partition size

Function	Command	Description
Partition Size Change Mode	CMD62(0xEFAC62EC)	Enter the Partition Size Change Mode
Partition Size Set Mode	CMD62(0x00CBAEA7)	Partition Size setting mode
Set Boot Partition Size	CMD62(BOOT_SIZE_MULTI)	Boot Partition Size value
Set RPMB Partition Size	CMD62(RPMB_SIZE_MULTI)	RPMB Partition Size value F/W Re-Partition is executed in this step.
Power Cycle		

Boot partition size is calculated as (128KB * BOOT_SIZE_MULTI)
The size of Boot Area Partition 1 and 2 can not be set independently. It is set as same value.

RPMB partition size is calculated as (128KB * RPMB_SIZE_MULTI).
In RPMB partition, CMD 0, 6, 8, 12, 13, 15, 18, 23, 25 are admitted.

Access Size of RPMB partition is defined as the below:

[Table 18] REL_WR_SEC_C value for write operation on RPMB partition

REL_WR_SEC_C	Description
REL_WR_SEC_C = 1	Access sizes 256B and 512B supported to RPMB partition
REL_WR_SEC_C > 1	Access sizes up to REL_WR_SEC_C * 512B supported to RPMB partition with 256B granularity

Any undefined set of parameters or sequence of commands results in failure access.

If the failure is in data programming case, the data is not programmed. And if the failure occurs in data read case, the read data is ‘0x00’.

5.1.1.2 Enhanced Partition (Area)

SAMSUNG e·MMC adopts Enhanced User Data Area as SLC Mode. Therefore when master adopts some portion as enhanced user data area in User Data Area, that area occupies double size of original set up size. (ex> if master set 1MB for enhanced mode, total 2MB user data area is needed to generate 1MB enhanced area)

Max Enhanced User Data Area size is defined as (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512kBytes)

5.1.2 Write protect management

In order to allow the host to protect data against erase or write, the device shall support write protect commands.

5.1.2.1 User Area Write Protection

TMP_WRITE_PROTECT (CSD[12]) and PERM_WRITE_PROTECT(CSD[13]) registers allow the host to apply write protection to whole device including Boot Partition, RPMB Partition and User Area.

[Table 19] whole device write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

USER_WP (EXT_CSD[171]) register allows the host to apply write protection to all the partitions in the user area.

[Table 20] User area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset
Temporary write protect	SET : Multiple programmable
	CLR : Multiple programmable

The host has the ability to check the write protection status of segments by using the SEND_WRITE_PROT_TYPE command (CMD31). When full card protection is enabled all the segments will be shown as having permanent protection.

5.1.2.2 Boot Partition Write Protection

BOOT_WP (EXT_CSD [173]) register allows the host to apply write protection to Boot Area Partitions.

[Table 21] Boot area write protect priority

Class	Setting
Permanent write protect	SET : One time programmable
	CLR : Not available
Power-on write protect	SET : One time programmable on power-on
	CLR : After power reset

An attempt to set both the disable and enable bit for a given protection mode (permanent or power-on) in a single switch command will have no impact and switch error occurs.
Setting both B_PERM_WP_EN and B_PWR_WP_EN will result in the boot area being permanently protected.

5.1.3 Boot operation

Device supports not only boot mode but also alternative boot mode.
Device supports high speed timing and dual data rate during boot

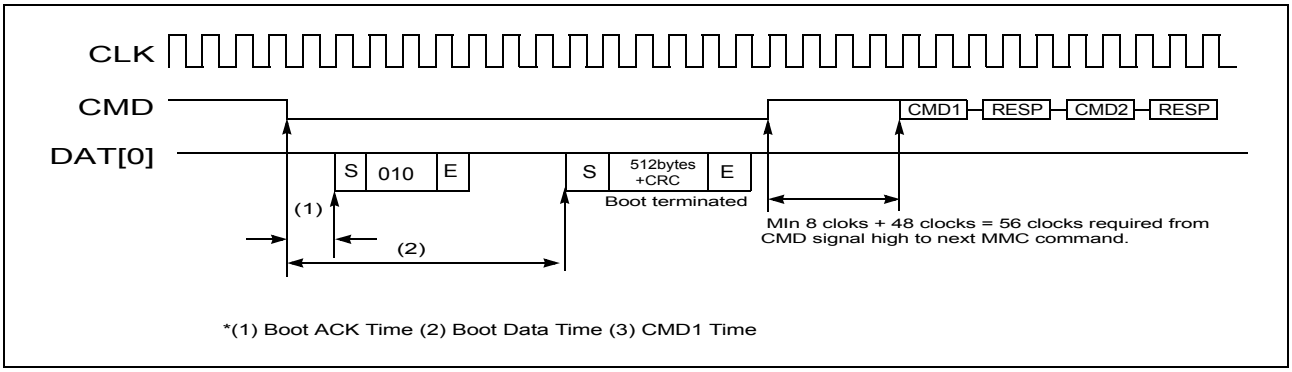


Figure 4. MultiMediaCard state diagram (boot mode)

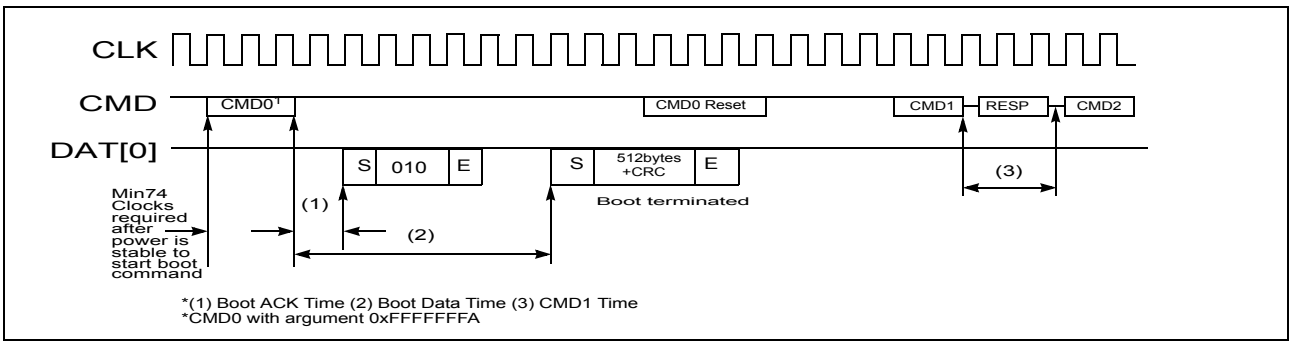


Figure 5. MultiMediaCard state diagram (alternative boot mode)

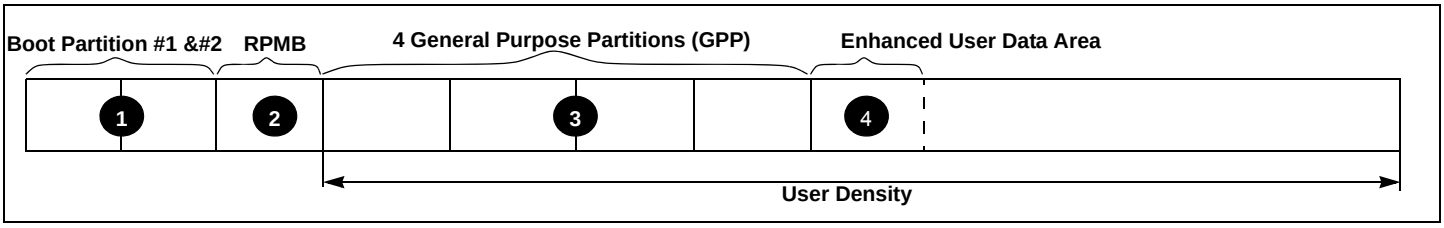
[Table 22] Boot ack, boot data and initialization Time

Timing Factor	Value
(1) Boot ACK Time	< 50 ms
(2) Boot Data Time	< 60 ms
(3) Initialization Time[1)]	< 3 secs

NOTE:
1) This initialization time includes partition setting, Please refer to INI_TIMEOUT_AP in 6.4 Extended CSD Register.
Normal initialization time (without partition setting) is completed within 1s (300ms for 4GB)

5.1.4 User Density

Total User Density depends on device type.
For example, 32MB in the SLC Mode requires 96MB in TLC.
This results in decreasing of user density



[Table 23] Capacity according to partition

	Boot partition 1	Boot partition 2	RPMB
Min.	2,048KB	2,048KB	128KB
Max.	4,096KB	4,096KB	4,096KB

[Table 24] Maximum Enhanced Partition Size

Device	Max. Enhanced Partition Size
4 GB	1,319,108,608 Bytes

[Table 25] User Density Size

Device	User Density Size
4 GB	3,959,422,976 Bytes

5.1.5 Auto Power Saving Mode

If host does not issue any command during a certain duration (1ms), after previously issued command is completed, the device enters "Power Saving mode" to reduce power consumption.

At this time, commands arriving at the device while it is in power saving mode will be serviced in normal fashion

[Table 26] Auto Power Saving Mode enter and exit

Mode	Enter Condition	Escape Condition
Auto Power Saving Mode	When previous operation which came from Host is completed and no command is issued during a certain time.	If Host issues any command

[Table 27] Auto Power Saving Mode and Sleep Mode

	Auto Power Saving Mode	Sleep Mode
NAND Power	ON	OFF
GotoSleep Time	< 1ms	< 1ms

5.1.6 Performance

[Table 28] Performance

Density	Sequential Read (MB/s)	Sequential Write (MB/s)
4 GB	71	7

* Test Condition : Bus width x8, 50MHz DDR, 512KB data transfer, w/o file system overhead, measured on Samsung's internal board

6.0 REGISTER VALUE

6.1 OCR Register

The 32-bit operation conditions register stores the VDD voltage profile of the e·MMC. In addition, this register includes a status information bit. This status bit is set if the e·MMC power up procedure has been finished. The OCR register shall be implemented by all e·MMCs.

[Table 29] OCR Register

OCR bit	VDD voltage window[2]	Register Value
[6:0]	Reserved	00 00000b
[7]	1.70 - 1.95	1b
[14:8]	2.0-2.6	000 0000b
[23:15]	2.7-3.6	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	00b (byte mode) 10b (sector mode) -[*Higher than 2GB only]
[31]	e·MMC power up status bit (busy)[1]	

NOTE :
1) This bit is set to LOW if the e·MMC has not finished the power up routine
2) The voltage for internal flash memory(VDDF) should be 2.7-3.6v regardless of OCR Register value.

6.2 CID Register

[Table 30] CID Register

Name	Field	Width	CID-slice	CID Value
Manufacturer ID	MID	8	[127:120]	0x15
Reserved		6	[119:114]	---
Card/BGA	CBX	2	[113:112]	01
OEM/Application ID	OID	8	[111:104]	---[1]
Product name	PNM	48	[103:56]	See Product name table
Product revision	PRV	8	[55:48]	---[2]
Product serial number	PSN	32	[47:16]	---[3]
Manufacturing date	MDT	8	[15:8]	---[4]
CRC7 checksum	CRC	7	[7:1]	---[5]
not used, always '1'	-	1	[0:0]	---

NOTE :
1),4),5) description are same as e.MMC JEDEC standard
2) PRV is composed of the revision count of controller and the revision count of F/W patch
3) 32-bit unsigned binary integer. (Random Number)

6.2.1 Product name table (In CID Register)

[Table 31] Product name

Part Number	Density	Product Name in CID Register (PNM)
KLM4G1YE4C-B0020YB	4 GB	0 x 4D3447315943

6.3 CSD Register

The Card-Specific Data register provides information on how to access the e·MMC contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows:
R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable.

[Table 32] CSD Register

Name	Field	Width	Cell Type	CSD-slice	CSD Value
					4GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	0x03
System specification version	SPEC_VERS	4	R	[125:122]	0x04
Reserved	-	2	R	[121:120]	-
Data read access-time 1	TAAC	8	R	[119:112]	0x27
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	0x01
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	0x32
Card command classes	CCC	12	R	[95:84]	0xF5
Max. read data block length	READ_BL_LEN	4	R	[83:80]	0x09
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0x00
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0x00
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0x00
DSR implemented	DSR_IMP	1	R	[76:76]	0x00
Reserved	-	2	R	[75:74]	-
Card size	C_SIZE	12	R	[73:62]	0xFFF
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	0x06
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	0x06
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	0x06
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	0x06
Card size multiplier	C_SIZE_MULT	3	R	[49:47]	0x07
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	0x1F
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	0x1F
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0x01
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	0x01
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0x00
Write speed factor	R2W_FACTOR	3	R	[28:26]	0x03
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	0x09
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0x00
Reserved	-	4	R	[20:17]	-
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0x00
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0x00
Copy flag (OTP)	COPY	1	R/W	[14:14]	0x01
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0x00
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0x00
File format	FILE_FORMAT	2	R/W	[11:10]	0x00
ECC code	ECC	2	R/W/E	[9:8]	0x00
CRC	CRC	7	R/W/E	[7:1]	-
Not used, always '1'	-	1	-	[0:0]	-

6.4 Extended CSD Register

The Extended CSD register defines the e·MMC properties and selected modes. It is 512 bytes long.
The most significant 320 bytes are the Properties segment, which defines the e·MMC capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the e·MMC is working in. These modes can be changed by the host by means of the SWITCH command.

R : Read only
W: One time programmable and not readable.
R/W: One time programmable and readable.
W/E : Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and not readable.
R/W/E: Multiple writable with value kept after power failure, H/W reset assertion and any CMD0 reset and readable.
R/W/C_P: Writable after value cleared by power failure and HW/ rest assertion (the value not cleared by CMD0 reset) and readable.
R/W/E_P: Multiple writable with value reset after power failure, H/W reset assertion and any CMD0 reset and readable.
W/E/_P: Multiple wtitable with value reset after power failure, H/W reset assertion and any CMD0 reset and not readable

[Table 33] Extended CSD Register

Name	Field	Size (Bytes)	Cell Type	CSD-slice	CSD Value
					4GB
Properties Segment					
Reserved[1]		7	-	[511:505]	-
Supported Command Sets	S_CMD_SET	1	R	[504]	0x01
HPI features	HPI_FEATURES	1	R	[503]	0x03
Background operations support	BKOPS_SUPPORT	1	R	[502]	0x01
Reserved[1]		255	-	[501:248]	-
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	[247]	Don't care
Background operations status	BKOPS_STATUS	1	R	[246]	0x00
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_-NUM	4	R	[245:242]	0x00
I st initialization time after partitioning	INI_TIMEOUT_AP	1	R	[241]	0x1E
Reserved[1]		1	-	[240]	-
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	[239]	0x00
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	[238]	0x00
Reserved[1]		2	-	[237:236]	-
Minimum Write Performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	[235]	0x00
Minimum Read Performance for 8 bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	[234]	0x00
Reserved[1]		1	-	[233]	-
TRIM Multiplier	TRIM_MULT	1	R	[232]	0x02
Secure Feature support	SEC_FEATURE_SUPPORT	1	R	[231]	0x15
Secure Erase Multiplier	SEC_ERASE_MULT	1	R	[230]	0x1B
Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	[229]	0x11
Boot information	BOOT_INFO	1	R	[228]	0x07
Reserved[1]		1	-	[227]	-
Boot partition size	BOOT_SIZE_MULTI	1	R	[226]	0x10
Access size	ACC_SIZE	1	R	[225]	0x05
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	[224]	0x01
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	[223]	0x01
Reliable write sector count	REL_WR_SEC_C	1	R	[222]	0x01
High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	[221]	0x02
Sleep current (VDDF)	S_C_VDDF	1	R	[220]	0x07
Sleep current (VDD)	S_C_VDD	1	R	[219]	0x07
Reserved[1]		1	-	[218]	-

Sleep/awake timeout	S_A_TIMEOUT	1	R	[217]	0x11
Reserved[1]		1	-	[216]	-
Sector Count	SEC_COUNT	4	R	[215:212]	0x760000
Reserved[1]		1	-	[211]	-
Minimum Write Performance for 8bit @52MHz	MIN_PERF_W_8_52	1	R	[210]	0x00
Minimum Read Performance for 8bit @52MHz	MIN_PERF_R_8_52	1	R	[209]	0x00
Minimum Write Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_W_8_26_4_52	1	R	[208]	0x00
Minimum Read Performance for 8bit @26MHz /4bit @52MHz	MIN_PERF_R_8_26_4_52	1	R	[207]	0x00
Minimum Write Performance for 4bit @26MHz	MIN_PERF_W_4_26	1	R	[206]	0x00
Minimum Read Performance for 4bit @26MHz	MIN_PERF_R_4_26	1	R	[205]	0x00
Reserved[1]		1	-	[204]	-
Power Class for 26MHz @ 3.6V	PWR_CL_26_360	1	R	[203]	0x00
Power Class for 52MHz @ 3.6V	PWR_CL_52_360	1	R	[202]	0x00
Power Class for 26MHz @ 1.95V	PWR_CL_26_195	1	R	[201]	0x00
Power Class for 52MHz @ 1.95V	PWR_CL_52_195	1	R	[200]	0x00
Partition switching timing	PARTITION_SWITCH_TIME	1	R	[199]	0x01
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	[198]	0x02
Reserved[1]		1	-	[197]	-
Card Type	CARD_TYPE	1	R	[196]	0x07
Reserved[1]		1	-	[195]	-
CSD Structure Version	CSD_STRUCTURE	1	R	[194]	0x02
Reserved[1]		1	-	[193]	-
Extended CSD Revision	EXT_CSD_REV	1	R	[192]	0x05
Modes Segment					
Command Set	CMD_SET	1	R/W/E_P	[191]	0x00
Reserved[1]		1	-	[190]	-
Command Set Revision	CMD_SET_REV	1	R	[189]	0x00
Reserved[1]		1	-	[188]	-
Power Class	POWER_CLASS	1	R/W/E_P	[187]	0x00
Reserved[1]		1	-	[186]	-
High Speed Interface Timing	HS_TIMING	1	R/W/E_P	[185]	0x00
Reserved[1]		1	-	[184]	-
Bus Width Mode	BUS_WIDTH	1	W/E_P	[183]	0x00
Reserved[1]		1	-	[182]	-
Erased Memory Content	ERASED_MEM_CONT	1	R	[181]	0x00
Reserved[1]		1	-	[180]	-
Partition configurationn	PARTITION_CONFIG	1	R/W/E& R/W/E_P	[179]	0x00
Boot config proteetion	BOOT_CONFIG_PRPT	1	R/W & R/W/C_P	[178]	0x00
Boot bus width1	BOOT_BUS_WIDTH	1	R/W/E	[177]	0x00
Reserved[1]		1	-	[176]	-
High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	[175]	0x00
Reserved[1]		1	-	[174]	-
Boot area write proection register	BOOT_WP	1	R/W & R/W/C_P	[173]	0x00
Reserved[1]		1	-	[172]	-

User area write protection register	USER_WP	1	R/W, R/W/ C_P& R/W/E_P	[171]	0x00
Reserved[1]		1	-	[170]	-
FW configuration	FW_CONFIG	1	R/W	[169]	0x00
RPMB Size	RPMB_SIZE_MULT	1	R	[168]	0x01
Write reliability setting register	WR_REL_SET	1	R/W	[167]	0x1F
Write reliability parameter register	WR_REL_PARAM	1	R	[166]	0x05
Reserved[1]		1	-	[165]	-
Manually start background operations	BKOPS_START	1	W/E_P	[164]	0x00
Enable background operations handshake	BKOPS_EN	1	R/W	[163]	0x00
H/W reset function	RST_n_FUNCTION	1	R/W	[162]	0x00
HPI management	HPI_MGMT	1	R/W/E_P	[161]	0x00
Partitoning support	RARTITIONING_SUPPORT	1	R	[160]	0x03
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	R	[159:157]	0x4EA
Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	[156]	0x00
Paritioning Setting	PARTITION_SETTING_COM-PLETED	1	R/W	[155]	0x00
General Purpose Partition Size	GP_SIZE_MULT	12	R/W	[154:143]	0x00
Enhanced User Data Area Size	ENH_SIZE_MULT	3	R/W	[142:140]	0x00
Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	[139:136]	0x00
Reserved[1]		1	-	[135]	-
Bad Block Management mode	SEC_BAD_BLK_MGMT	1	R/W	[134]	0x00
Reserved[1]		6	-	[133:128]	-
Vendor Config	VENDOR_CONFIG	60	-	[127:68]	Don't care
Vendor Config (Auto Background Operation)	AUTO_BKOPS	1	R/W/E	[67]	Don't care
Vendor Config (Aligned Optimal Trim/Discard Size)	ALIGNED_OPTIMAL_TRIM_ DISCARD_SIZE	1	R	[66]	0x08
Vendor Config (Optimized Features)	OPTIMIZED_FEATURES	2	R	[65:64]	0x03
Reserved[1]		29	-	[63:35]	-
Power Off Notification	POWER_OFF_NOTIFICATION	1	R/W/E_P	[34]	Don't care
Reserved[1]		34	-	[33:0]	-

NOTE :
1) Reserved bits should be read as "0."

7.0 AC PARAMETER

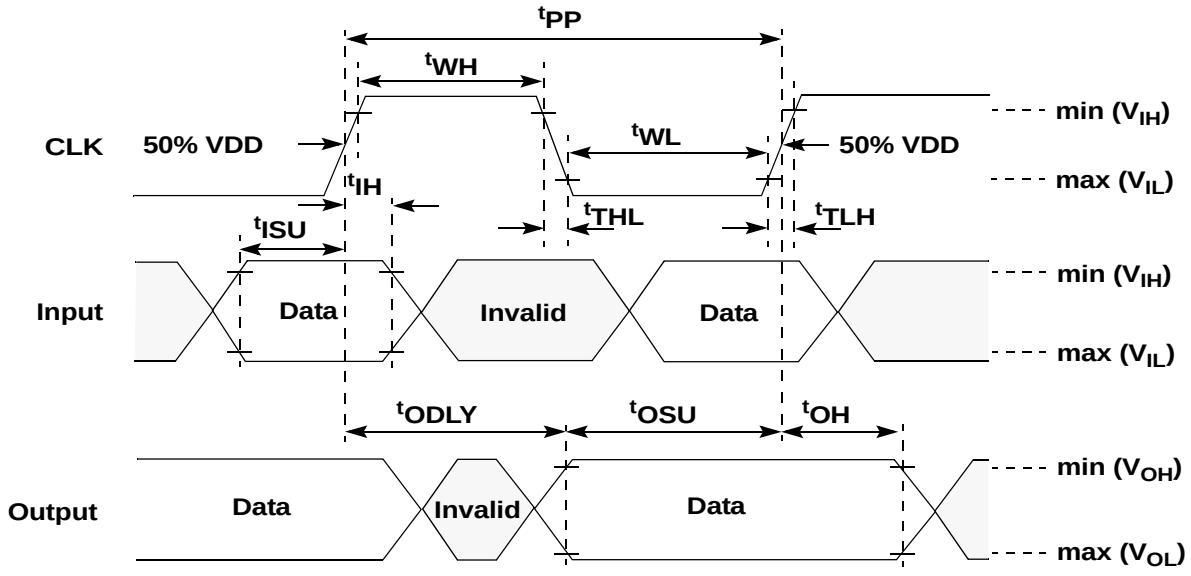
7.1 Time Parameter

[Table 34] Time Parameter

Timing Paramter		Max. Value	Unit
Initialization Time (tINIT)	Normal [1]	1 (300ms for 4GB)	ms
	After partition setting [2]	3	s
Read Timeout		100	ms
Write Timeout		350	ms
Erase Timeout		15	ms
Force Erase Timeout		3	min
Secure Erase Timeout		8	s
Secure Trim step1 Timeout		5	s
Secure Trim step2 Timeout		3	s
Trim Timeout [3]		600	ms
Partition Switching Timeout (after Init)		100	us
Discard Timeout		15	ms

NOTE:
1) Normal Initialization Time without partition setting
2) Initialization Time after partition setting, refer to INI_TIMEOUT_AP in 6.4 EXT_CSD register
3) If 8KB Size and Address are aligned, Max. Timeout value is 300ms
4) Power Off Notification is not implemented for 4,8GB Products

7.2 Bus Timing Parameter



Data must always be sampled on the rising edge of the clock.

Figure 6. Bus signal levels

[Table 35] Default (under 26MHz)

Parameter	Symbol	Min	Max	Unit	Remark[1]
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[2]					
Clock frequency Data Transfer Mode3	fPP	0[4]	26	MHz	CL <= 30 pF
Clock frequency Identification Mode	f_{OD}	0[4]	400	kHz	
Clock low time	t_{WL}	10		ns	C_L <= 30 pF
Clock high time	t_{WH}	10			C_L <= 30 pF
Clock rise time[5]	t_{TLH}		10	ns	C_L <= 30 pF
Clock fall time	t_{THL}		10	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output hold time	t_{OH}	8.3		ns	CL <= 30 pF
Output set-up time	t_{OSU}	11.7		ns	CL <= 30 pF

NOTE :
1) Device must always start with the backward-compatible interface timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2) CLK timing is measured at 50% of VDD.
3) For compatibility with cards that suport the v4.2 standard or earlier verison, host should not use>26MHz before switching to high-speed interface timing.
4) Frequency is periodically sampled and is not 100% tested.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).

[Table 36] High-Speed Mode

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK(All values are referred to min(V_{IH}) and max(V_{IL})[1]					
Clock frequency Data Transfer Mode[2]	f_{PP}	0[3]	52[4)]	MHz	C_L <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode	f_{OD}	0[3]	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock High time	t_{WH}	6.5		ns	C_L <= 30 pF
Clock rise time[5]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		13.7	ns	CL <= 30 pF
Output hold time	t_{OH}	2.5			C_L <= 30 pF
Signal rise time	t_{RISE}		3	ns	C_L <= 30 pF
Signal fall time	t_{FALL}		3	ns	C_L <= 30 pF

NOTE :
1) CLK timing is measured at 50% of VDD.
2) A MultiMediaCard shall support the full frequency range from 0-26MHz, or 0-52MHz
3) Frequency is periodically sampled and is not 100% tested.
4) Device can operate as high-speed card interface timing at 26MHz clock frequency.
5) CLK rise and fall times are measured by min(V_{IH}) and max(V_{IL}).6) Inputs CMD, DAT rise and fall times are measured by min(V_{IH}) and max(V_{IL}), and outputs CMD, DAT rise and fall times are measured by min(V_{OH}) and max(V_{OL}).

7.3 Bus timing for DAT signals during 2x data rate operation

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK.The CMD signal still operates synchronously of the rising edge of CLK and there fore it complies with the bus timing specified in chapter 7.2, Therefore there is no timing change for the CMD signal

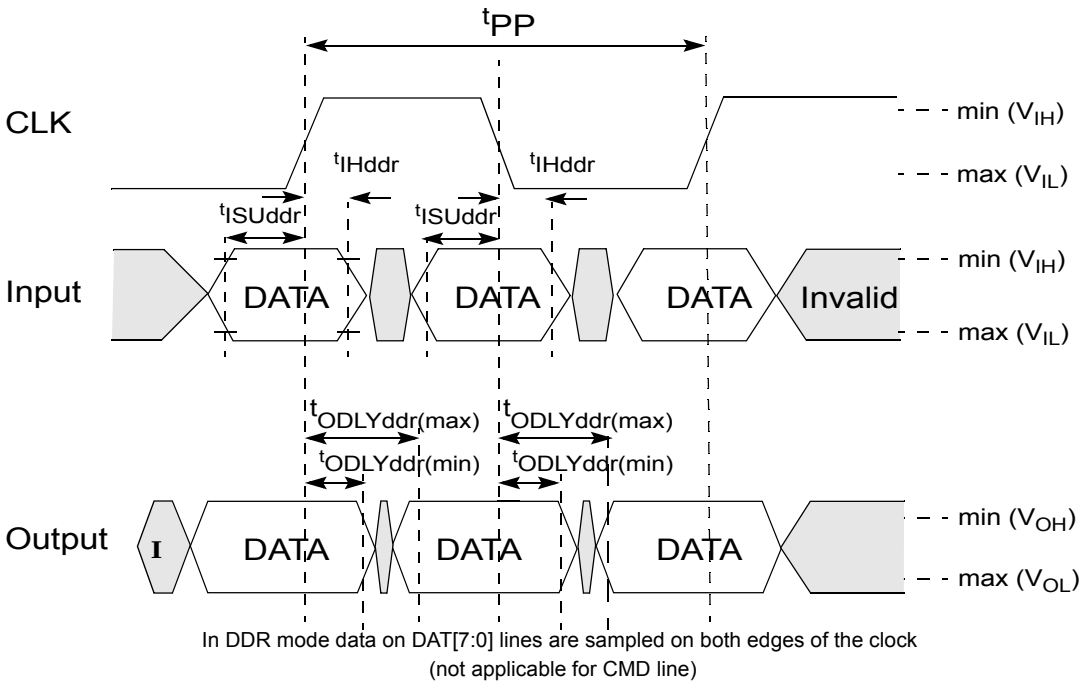


Figure 7. Timing diagram: data input/output in dual data rate mode

7.3.1 Dual data rate interface timings

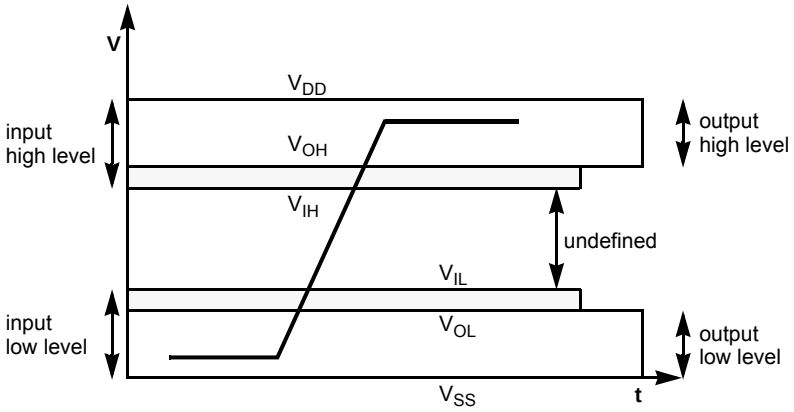
[Table 37] High-speed dual rate interface timing

Parameter	Symbol	Min	Max.	Unit	Remark[1]
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

NOTE :
1) CLK timing is measuted at 50% of VDD
2) Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max(V_{IL}), and outputs CMD,DATrise and fall times measured by min(V_{OH}) and max(V_{OL})

7.4 Bus signal levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



7.4.1 Open-drain mode bus signal level

[Table 38] Open-drain bus signal level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.2		V	Note 1)
Output LOW voltage	V_{OL}		0.3	V	I_{OL} = 2 mA

Note:

1) Because Voh depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet Voh Min value.
The input levels are identical with the push-pull mode bus signal levels.

7.4.2 Push-pull mode bus signal level.high-voltage MultiMediaCard

To meet the requirements of the JEDEC standard JESD8C.01, the card input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range:

[Table 39] Push-pull signal level.high-voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -100 uA@V_{DD} min
Output LOW voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 100 uA@V_{DD} min
Input HIGH voltage	V_{IH}	0.625*V_{DD}	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.25*V_{DD}	V	

7.4.3 Push-pull mode bus signal level.dual-voltage MultiMediaCard

The definition of the I/O signal levels for the Dual voltage MultiMediaCard changes as a function of V_{DD}.

- 2.7V - 3.6V: Identical to the High Voltage MultiMediaCard (refer to Chapter 7.4.2 on page25 above).
- 1.95V - 2.7V: Undefined. The card is not operating at this voltage range.
- 1.70V - 1.95V: Compatible with EIA/JEDEC Standard “EIA/JESD8-7 Normal Range” as defined in the following table.

[Table 40] Push-pull signal level—dual-voltage MultiMediaCard

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	V_{OH}	V_{DD} - 0.45V		V	I_{OH} = -2mA
Output LOW voltage	V_{OL}		0.45V	V	I_{OL} = 2mA
Input HIGH voltage	V_{IH}	0.65*V_{DD} 1)	V_{DD} + 0.3	V	
Input LOW voltage	V_{IL}	V_{SS} - 0.3	0.35*V_{DD} 2)	V	

NOTE:
1) 0.7*V_{DD} for MMC4.3 and older revisions.
2) 0.3*V_{DD} for MMC4.3 and older revisions.

8.0 DC PARAMETER

8.1 Active Power Consumption during operation

[Table 41] Active Power Consumption during operation

Density	NAND Type	CTRL	NAND	Unit
4 GB	32Gb TLC x 1	100	50	mA

* Power Measurement conditions: Bus configuration =x8 @52MHz
* The measurement for max RMS current is the average RMS current consumption over a period of 100ms.

8.2 Standby Power Consumption in auto power saving mode and standby state

[Table 42] Standby Power Consumption in auto power saving mode and standby state

Density	NAND Type	CTRL		NAND		Unit
		25°C(Typ)	85°C	25°C(Typ)	85°C	
4 GB	32Gb TLC x 1	100	250	40	85	uA

NOTE:
Power Measurement conditions: Bus configuration =x8 , No CLK
*Typical value is measured at Vcc=3.3V, TA=25°C. Not 100% tested.

8.3 Sleep Power Consumption in Sleep State

[Table 43] Sleep Power Consumption in Sleep State

Density	NAND Type	CTRL		NAND	Unit
		25°C(Typ)	85°C		
4 GB	32Gb TLC x 1	100	250	0[1)]	uA

NOTE:
Power Measurement conditions: Bus configuration =x8 , No CLK
1) In auto power saving mode , NAND power can not be turned off .However in sleep mode NAND power can be turned off. If NAND power is alive , NAND power is same with that of the Standby state.

8.4 Supply Voltage

[Table 44] Supply Voltage

Item	Min	Max	Unit
VDD	1.70 (2.7)	1.95 (3.6)	V
VDDF	2.7	3.6	V
Vss	-0.5	0.5	V

8.5 Bus Operating Conditions

[Table 45] Bus Operating Conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	V_{CCQ} + 0.5	V
Input Leakage Current	-2	2	μA
Output Leakage Current	-2	2	μA

8.6 Bus Signal Line Load

The total capacitance C_L of each line of the e·MMC bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of the e·MMC connected to this line:

$$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$$

The sum of the host and bus capacitances should be under 20pF.

[Table 46] Bus Signal Line Load

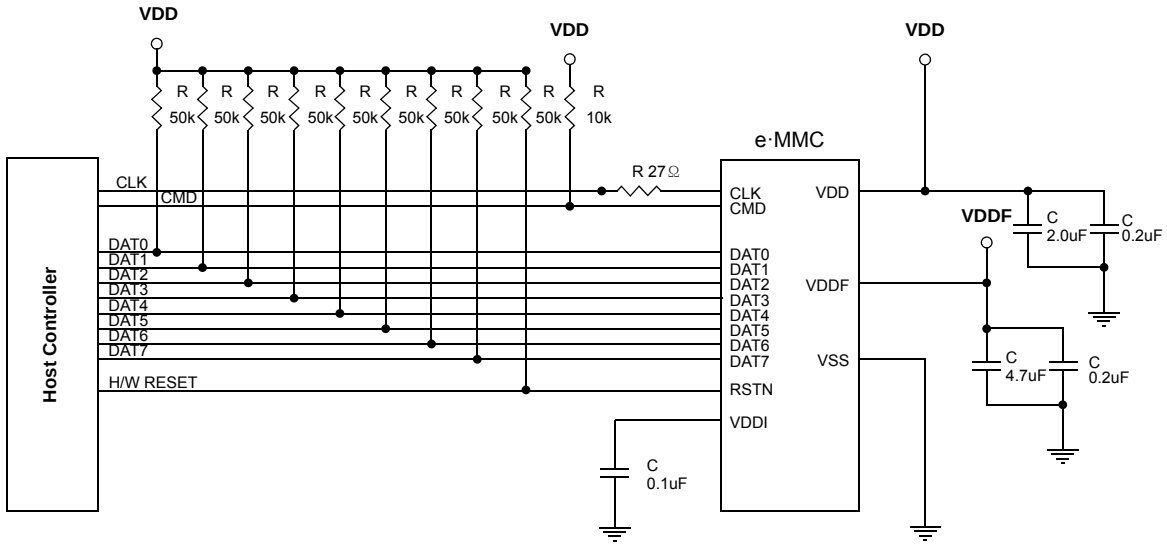
Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7		100	KOhm	to prevent bus floating
Pull-up resistance for DAT0-DAT7	R_{DAT}	10		100	KOhm	to prevent bus floating
Internal pull up resistance DAT1-DAT7	R_{int}	10		150	KOhm	to prevent unconnected lines floating
Single e·MMC capacitance	C_{BGA}		7	12	pF	
Maximum signal line inductance				16	nH	f_{PP} <= 52 MHz

A. e·MMC Connection Guide

This connection guide is an example for customers to adopt e·MMC more easily

- This appendix is just guideline for e·MMC connection. This value and schematic can be changed depending on the system environment.
- Coupling capacitor should be connected with VDD and VSS as close as possible.
- VDDI Capacitor is min 0.1uF
- Impedance on CLK match is needed.
- SAMSUNG recommends 27Ω for resistance on CLK line. However 0Ω ~47Ω is also available.
- If host does not have a plan to use H/W reset, it is not needed to put 50KΩ pull-up resistance on H/W reset line.
- SAMSUNG recommends user separate VDD and VDDF power.

A.1 x8 support Host connection Guide



A.2 x4 support Host connection Guide