SAMSUNG

Rev. 1.0, Aug. 2021

K4UBE3D4AB

32Gb DDP LPDDR4X SDRAM

200FBGA, 10x15
128Mb x16DQ x8banks x2channels

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Datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
0.0	- First version for target specification.	Oct 21st, 2020	Target	J.Y.Bae
0.5	- Preliminary datasheet. - Update IDD spec values. - Correct ZQ connection in functional block diagram.	Jul 5th, 2021	Preliminary	J.Y.Bae
1.0	- Final datasheet.	Aug 23rd, 2021	Final	J.Y.Bae

Table Of Contents

32Gb DDP LPDDR4X SDRAM

1.0 COMPARISION BETWEEN LPDDR3, LPDDR4 AND LPDDR4X

	Items	LPDDR3	LPDDR4	LPDDR4X
Feature	CLK scheme	Differential (CLK/CLKB)	←	←
	Data scheme	DDR Single-ended, Bi-Directional	←	←
	DQS scheme	Differential (DQS/DQSB), Bi-Directional	←	←
	ADD / CMD scheme	DDR	SDR	SDR
	State Diagram	Refer to the Datasheet	Refer to the Datasheet	Refer to the Datasheet
	Command Truth Table	No support BST	Refer to the Datasheet	Refer to the Datasheet
	Data mask Truth Table	As is	←	←
	I/O Interface	HSUL_12	LVSTL_11	LVSTLE_06
	Burst Length	8	16, 32(OTF)	16, 32(OTF)
	Burst Type	Sequential	←	←
	No Wrap	No support	←	←
	# of Bank per channel	8	←	←
	Organization per channel	x16/x32	x8, x16	x8, x16
	Data Mask	Support (Write)	Support (Masked Write)	Support (Masked Write)
	Refresh mode	Auto / Self Refresh	←	←
	Masked Write	N/A	Support	Support
	DBI	N/A	Support	Support
Addressing	Row	Refer to the Datasheet (CA0 ~ CA9 1clock DDR based)	Refer to the datasheet (CA0 ~ CA5 4clock SDR based)	Refer to the datasheet (CA0 ~ CA5 4clock SDR based)
	Column			
	Bank			
	Refresh Requirements			
AC Parameter	Speed bin [Mbps]	1600/1866	3200/3733/4266	3200/3733/4266
	Read/Write latency	Refer to the Datasheet	Refer to the datasheet	Refer to the datasheet
	Core Parameters			
	IO Parameters			
	CA / CS / Setup / Hold / Deratin			
	Data Setup / Hold / Deratin			
Special Function	PASR	Support	←	←
	TCSR	Support	←	←
	Deep Power Down	No Support	N/A	N/A
	Configurable D/S	Support	←	←
	ZQ Calibration	Support	←	←
	DQ Calibration	Support1)	Refer to the datasheet	Refer to the datasheet
	CA Calibration	Support	←	←
	Write Leveling	Support	←	←
Power Supply	VDD1 [V]	1.70 ~ 1.95	←	←
	VDD2 [V]	1.14 ~ 1.30	1.06 ~ 1.17	1.06 ~ 1.17
	VDDQ [V]	1.14 ~ 1.30	1.06 ~ 1.17	0.57 ~ 0.65
	VDDCA [V]	1.14 ~ 1.30	N/A	N/A
IDD Specification Parameters and Test Conditions	IDD Measurement Conditions	As is	BL16 based	BL16 based
	IDD Specification	As is	Refer to the datasheet	Refer to the datasheet
Temperature	General ['C]	-25 ~ 85	←	←

		Items	LPDDR3	LPDDR4	LPDDR4X
Pull-down Pull-up Characteristics		w/ ZQ Calibration	As is	←	←
		w/o ZQ Calibration	As is	←	←
		w/ V_{OH} Calibration	N/A	Support	Support
		w/o V_{OH} Calibration	N/A	Support	Support
		Temperature and Voltage Sensitivity	As is	←	←
		RZQI-V Curve	As is	←	←
Input/Output Capacitance[1]			Refer to the Datasheet	Refer to the Datasheet	Refer to the Datasheet
Absolute maximum DC ratings		VDD1 [V]	-0.4 ~ 2.3	-0.4 ~ 2.1	←
		VDD2 [V]	-0.4 ~ 1.6	-0.4 ~1.4	←
		VDDQ [V]	-0.4 ~ 1.6	-0.4 ~ 1.4	←
		VDDCA [V]	-0.4 ~ 1.6	N/A	N/A
		VIN/VOUT [V]	-0.4 ~ 1.6	-0.4 ~ 1.4	←
		Tstg ['C]	-55 ~ 125	←	←
		Input leakage [uA]	As is	-2 ~ 2	-2 ~ 2
Input/Output Operating condition	AC/DC Logic Input Levels for Single-ended Signals	CA and CS pins	AC : VREF ± 0.150V / ± 0.135V (1600/1866) DC : VREF ± 0.10V/0.10V (1600/1866)	VREF(CA), Internal VREF	VREF(CA), Internal VREF
		CKE pin	0.65×VDDCA ~ 0.35×VDDCA	AC : 0.75×VDD2 @ Min VDD2+0.2 @ Max DC : 0.65×VDD2 @ Min VDD2+0.2 @ Max	AC : 0.75×VDD2@Min VDD2+0.2@Max DC : 0.65×VDD2@Min VDD2+0.2@Min
		DQ pins	AC : VREF ± 0.15V/0.135V (1600/1866) DC : VREF ± 0.10V/0.10V (1600/1866)	VREF(DQ), Internal VREF	VREF(DQ), Internal VREF
		VREF_CA/DQ tolerance	0.49×VDDQ ~ 0.51×VDDQ	Internal VREF	Internal VREF
	AC/DC Logic Input Levels for Differential	VIHdiff/VILdiff (AC/DC) tDVAC	As is	TBD	TBD
		VSEH/VSEL(AC)	As is	TBD	TBD
	Differential Input Cross Point Voltage	VIXCA/VIXDQ	As is	TBD	TBD
	Slew Rate definitions for Differential	VILdiff /VIHdiff (Max/Min)	As is	TBD	TBD
	AC/DC Output levels for Differential	VOHdiff / VOLdiff (AC)	As is	TBD	TBD
		IOZ	As is	-5 ~ 5	-5 ~ 5
		MMPUPD	As is	TBD	TBD
	Single ended output Slew	VOH/VOL(AC/DC)	As is	TBD	TBD
		SRQse	As is	3.5 ~ 9.0	3.0 ~ 9.0
	Differential Output Slew	VOHdiff/VOLdiff(AC)	As is	TBD	TBD
		SRQdiff	As is	7.0 ~ 18.0	6.0 ~ 18.0
	Overshoot / Undershoot	Maximum Amplitude	As is	←	←
		Maximum Area	VDD/VSS : 0.1[V-ns]	←	←
	Driver Output Timing		HSUL_12	LVSTL_11	LVSTLE_06

NOTE:
1) The parameter applies to both die and package.

LPDDR4X SDRAM SPECIFICATION

32Gb DDP = 128M x16DQ x8banks x2channels
200FBGA, 10x15 Package

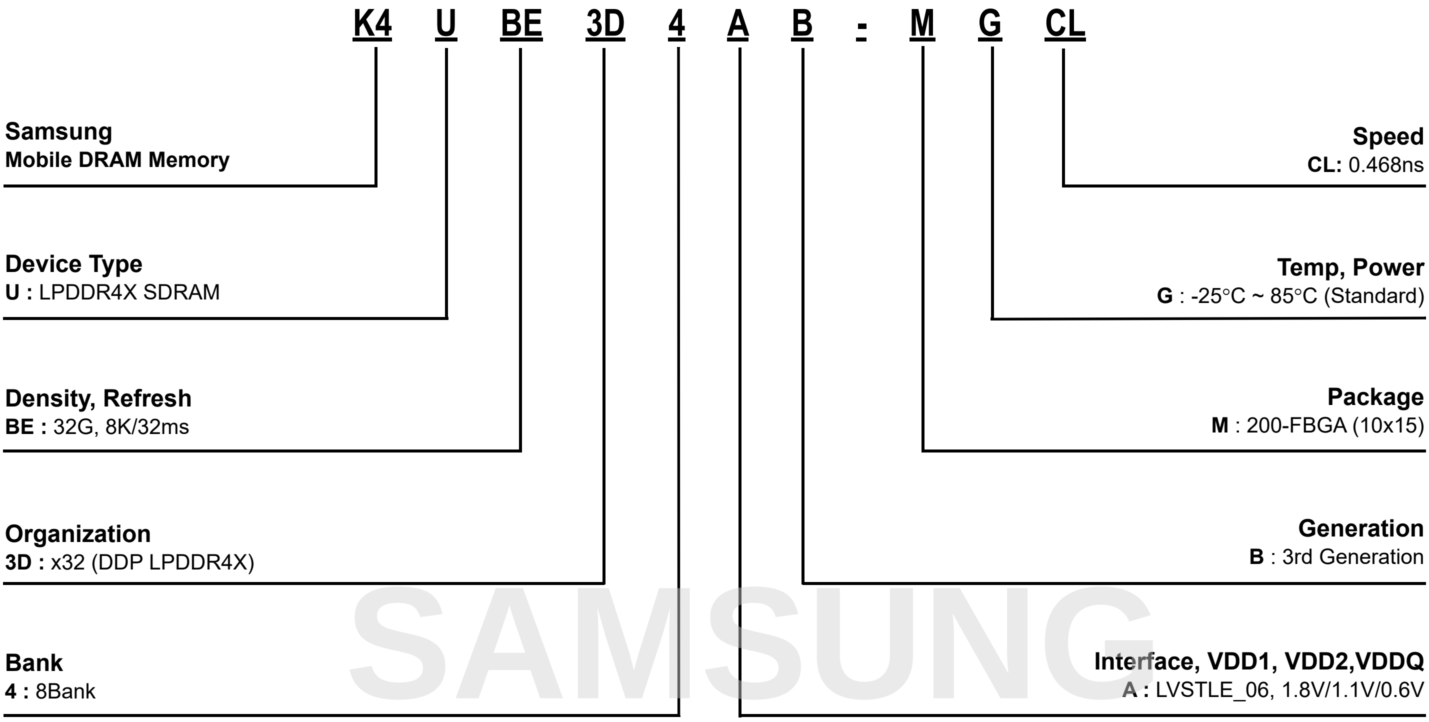
2.0 KEY FEATURE

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS_t, DQS_c), These are transmitted/received with data to be used in capturing data at the receiver
- Differential clock inputs (CK_t and CK_c)
- Differential data strobes (DQS_t and DQS_c)
- Commands & addresses entered positive CK edges; data and data mask referenced to both edges of DQS
- 2channel composition per die
- 8 internal banks for each channel
- DMI Pin : DBI (Data Bus Inversion) when normal write and read operation, Data mask (DM) for masked write when DBI off
  - Counting # of DQ's 1 for masked write when DBI on
- Burst Length: 16, 32 (OTF)
- Burst Type: Sequential
- Read & Write latency : Refer to Table 13.4 AC Timing
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Refresh and Self Refresh Modes
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Write Leveling
- CA Calibration
- Internal VREF and VREF training
- FIFO based write/read training
- MPC (Multi Purpose Command)
- LVSTLE (Low Voltage Swing Terminated Logic Extension) IO
- VDD1/VDD2/VDDQ : 1.8V/1.1V/0.6V
- VSSQ Termination
- No DLL : CK to DQS is not synchronized
- Edge aligned data output, write training for data input center align
- Refresh rate : 3.9us

3.0 ORDERING INFORMATION

Part No.	Org.	Package	Temperature	Max Frequency	Interface
K4UBE3D4AB-MGCL	2Ch, x16/Ch	10x15, 200-FBGA	Tc = -25 ~ 85°C	4266Mbps (tCK=0.468ns)	LVSTLE_06

NOTE :
1) 4266Mbps is backward compatible to lower frequency.



Samsung
Mobile DRAM Memory

Device Type
U : LPDDR4X SDRAM

Density, Refresh
BE : 32G, 8K/32ms

Organization
3D : x32 (DDP LPDDR4X)

Bank
4 : 8Bank

Speed
CL: 0.468ns

Temp, Power
G : -25°C ~ 85°C (Standard)

Package
M : 200-FBGA (10x15)

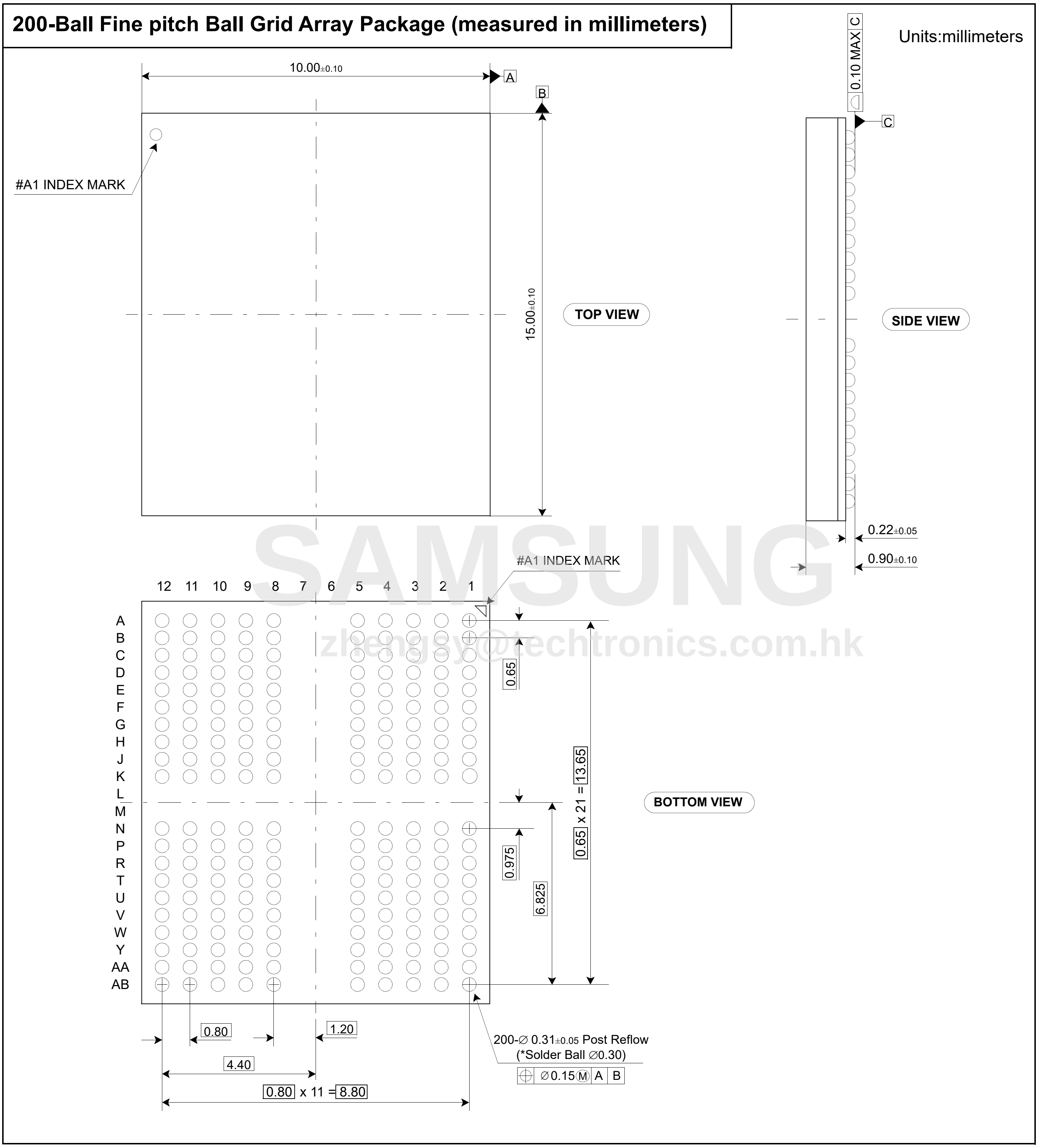
Generation
B : 3rd Generation

Interface, VDD1, VDD2,VDDQ
A : LVSTLE_06, 1.8V/1.1V/0.6V

4.0 PACKAGE DIMENSION & PIN DESCRIPTION

4.1 LPDDR4X SDRAM Package Dimension

200-Ball Fine pitch Ball Grid Array Package (measured in millimeters)



4.2 LPDDR4X SDRAM Package Ballout

200Ball FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	VSS	VDD2	ZQ0	NB	NB	ZQ1	VDD2	VSS	DNU	DNU
B	DNU	DQ0_a	VDDQ	DQ7_a	VDDQ	NB	NB	VDDQ	DQ15_a	VDDQ	DQ8_a	DNU
C	VSS	DQ1_a	DMI0_a	DQ6_a	VSS	NB	NB	VSS	DQ14_a	DMI1_a	DQ9_a	VSS
D	VDDQ	VSS	DQS0_t_a	VSS	VDDQ	NB	NB	VDDQ	VSS	DQS1_t_a	VSS	VDDQ
E	VSS	DQ2_a	DQS0_c_a	DQ5_a	VSS	NB	NB	VSS	DQ13_a	DQS1_c_a	DQ10_a	VSS
F	VDD1	DQ3_a	VDDQ	DQ4_a	VDD2	NB	NB	VDD2	DQ12_a	VDDQ	DQ11_a	VDD1
G	VSS	ODT_CA_a1),2)	VSS	VDD1	VSS	NB	NB	VSS	VDD1	VSS	DNU	VSS
H	VDD2	CA0_a	CS1_a	CS0_a	VDD2	NB	NB	VDD2	CA2_a	CA3_a	CA4_a	VDD2
J	VSS	CA1_a	VSS	CKE0_a	CKE1_a	NB	NB	CK_t_a	CK_c_a	VSS	CA5_a	VSS
K	VDD2	VSS	VDD2	VSS	DNU	NB	NB	DNU	VSS	VDD2	VSS	VDD2
L	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB
M	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB	NB
N	VDD2	VSS	VDD2	VSS	DNU	NB	NB	DNU	VSS	VDD2	VSS	VDD2
P	VSS	CA1_b	VSS	CKE0_b	CKE1_b	NB	NB	CK_t_b	CK_c_b	VSS	CA5_b	VSS
R	VDD2	CA0_b	CS1_b	CS0_b	VDD2	NB	NB	VDD2	CA2_b	CA3_b	CA4_b	VDD2
T	VSS	ODT_CA_b1),2)	VSS	VDD1	VSS	NB	NB	VSS	VDD1	VSS	RESET_n	VSS
U	VDD1	DQ3_b	VDDQ	DQ4_b	VDD2	NB	NB	VDD2	DQ12_b	VDDQ	DQ11_b	VDD1
V	VSS	DQ2_b	DQS0_c_b	DQ5_b	VSS	NB	NB	VSS	DQ13_b	DQS1_c_b	DQ10_b	VSS
W	VDDQ	VSS	DQS0_t_b	VSS	VDDQ	NB	NB	VDDQ	VSS	DQS1_t_b	VSS	VDDQ
Y	VSS	DQ1_b	DMI0_b	DQ6_b	VSS	NB	NB	VSS	DQ14_b	DMI1_b	DQ9_b	VSS
AA	DNU	DQ0_b	VDDQ	DQ7_b	VDDQ	NB	NB	VDDQ	DQ15_b	VDDQ	DQ8_b	DNU
AB	DNU	DNU	VSS	VDD2	VSS	NB	NB	VSS	VDD2	VSS	DNU	DNU

[Top View]

🟦	Channel A	🟪	Channel B
🟥	Power	🟩	Ground
🟦	ODT_CA	🟫	RESET_n
🟨	ZQ	⬛	NB
⬜	DNU		

NOTE :
1) ODT(CA)_[x] balls are wired to ODT(CA)_[x] pads of Rank 0 DRAM die. ODT(CA)_[x] pads for other ranks (if present) are disabled in the package.
2) For the LPDDR4X, ODT_Bond pad is ignored. ODT pin should connect to VDD2 or VSS.

4.3 PAD Definition And Description

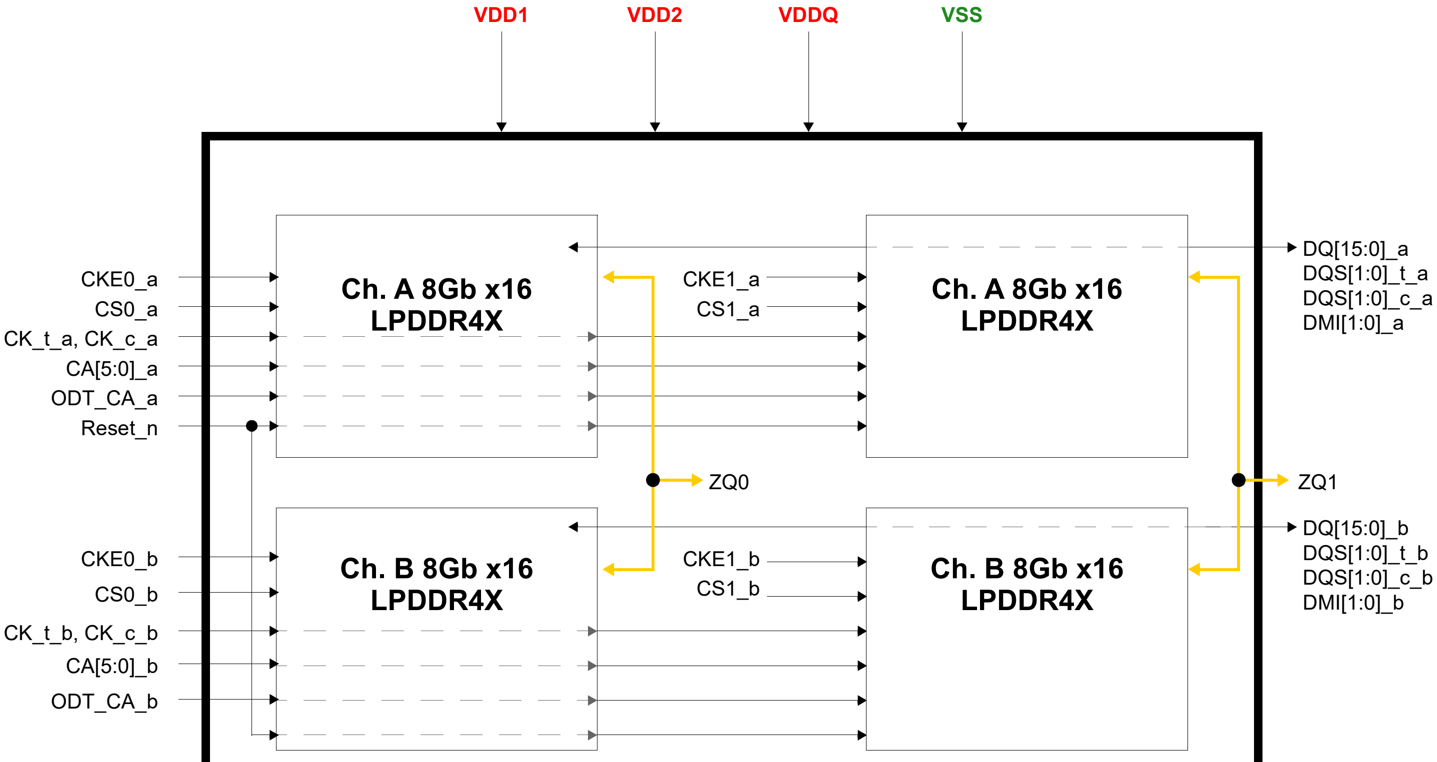
Pin Name	Pin Function Channel-A
CK_t_a, CK_c_a	System Differential Clock
CKE0_a, CKE1_a	Clock Enable
CS0_a, CS1_a	Chip Select
CA[5:0]_a	DDR Command / Address Inputs
DMI[1:0]_a	Input Data Inversion
DQS[1:0]_t_a	Data Strobe Bi-directional
DQS[1:0]_c_a	Data Strobe Complementary
DQ[15:0]_a	Data Inputs / Outputs
ODT_CA_a	On die termination

Pin Name	Pin Function Channel-B
CK_t_b, CK_c_b	System Differential Clock
CKE0_b, CKE1_b	Clock Enable
CS0_b, CS1_b	Chip Select
CA[5:0]_b	DDR Command / Address Inputs
DMI[1:0]_b	Input Data Inversion
DQS[1:0]_t_b	Data Strobe Bi-directional
DQS[1:0]_c_b	Data Strobe Complementary
DQ[15:0]_b	Data Inputs / Outputs
ODT_CA_b	On die termination

Pin Name	Pin Function Common
DNU	Do Not Use
NC	No Connect

Pin Name	Pin Function Common
VDD1	Core Power Supply 1
VDD2	Core Power Supply 2
VDDQ	I/O Power Supply
VSS	Ground
ZQ0, ZQ1	Reference Pin for Output Driver Strength Calibration
RESET_n	RESET

4.4 Functional Block Diagram



4.5 LPDDR4X Pad Definition and Description

4.5.1 Dual channel per die device

[Table 1] Pad Definition and Description for Dual channel

Symbol	Type	Description
CK_t_A CK_c_A CK_t_B CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A CKE_B	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A, CS_B	Input	**Chip Select:** CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A CA[5:0]_B	Input	**Command/Address Inputs:** CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**CA ODT Control:** The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins.
DQ[15:0]_A DQ[15:0]_B	I/O	**Data Inputs/Outputs:** Bi-direction data bus
DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B	I/O	**Data Strobe:** DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A DMI[1:0]_B	I/O	**Data Mask Inversion:** DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	**Calibration Reference:** Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor.
VDDQ,VDD1, VDD2	Supply	**Power Supplies:** Isolated on the die for improved noise immunity.
V_{SS}, V_{SSQ}	GND	**Ground Reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

NOTE :
1) "_A" and "_B" indicate DRAM channel "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only.

5.0 FUNCTIONAL DESCRIPTION

LPDDR4X-SDRAM is a high-speed synchronous DRAM device internally configured with 2 channels. Dual channel is comprised of 8-banks with from 2Gb to 16Gb per channel density. The configuration for channel density that is greater than 16Gb is still TBD[1].

This device contains the following number of bits:
Dual-channel SDRAM devices contain the following number of bits:
16Gb has 17,179,869,184 bits

LPDDR4X devices use a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See command truth table for details.

These devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4X SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4X SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4X SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

5.1 LPDDR4X SDRAM Addressing

[Table 2] LPDDR4X SDRAM x16 mode Addressing for Dual Channel SDRAM Device

Memory Density (per Die)		16Gb
Memory Density (per x16 channel)		8Gb
Configuration		64Mb x 16DQ x 8 banks x 2 channels
Number of Channels (per die)		2
Number of Banks (per channel)		8
Array Pre-Fetch (bits, per channel)		256
Number of Rows (per Channel)		65,536
Number of Columns (fetch boundaries)		64
Page Size (Bytes)		2048
Channel Density (Bits per channel)		8,589,934,592
Total Density (Bits per die)		17,179,869,184
Bank Addresses		BA0-BA2
x16	Row Addresses [2]	R0 - R15
	Column Addresses [1], [2]	C0-C9
Burst Starting Address Boundary		64 - bit

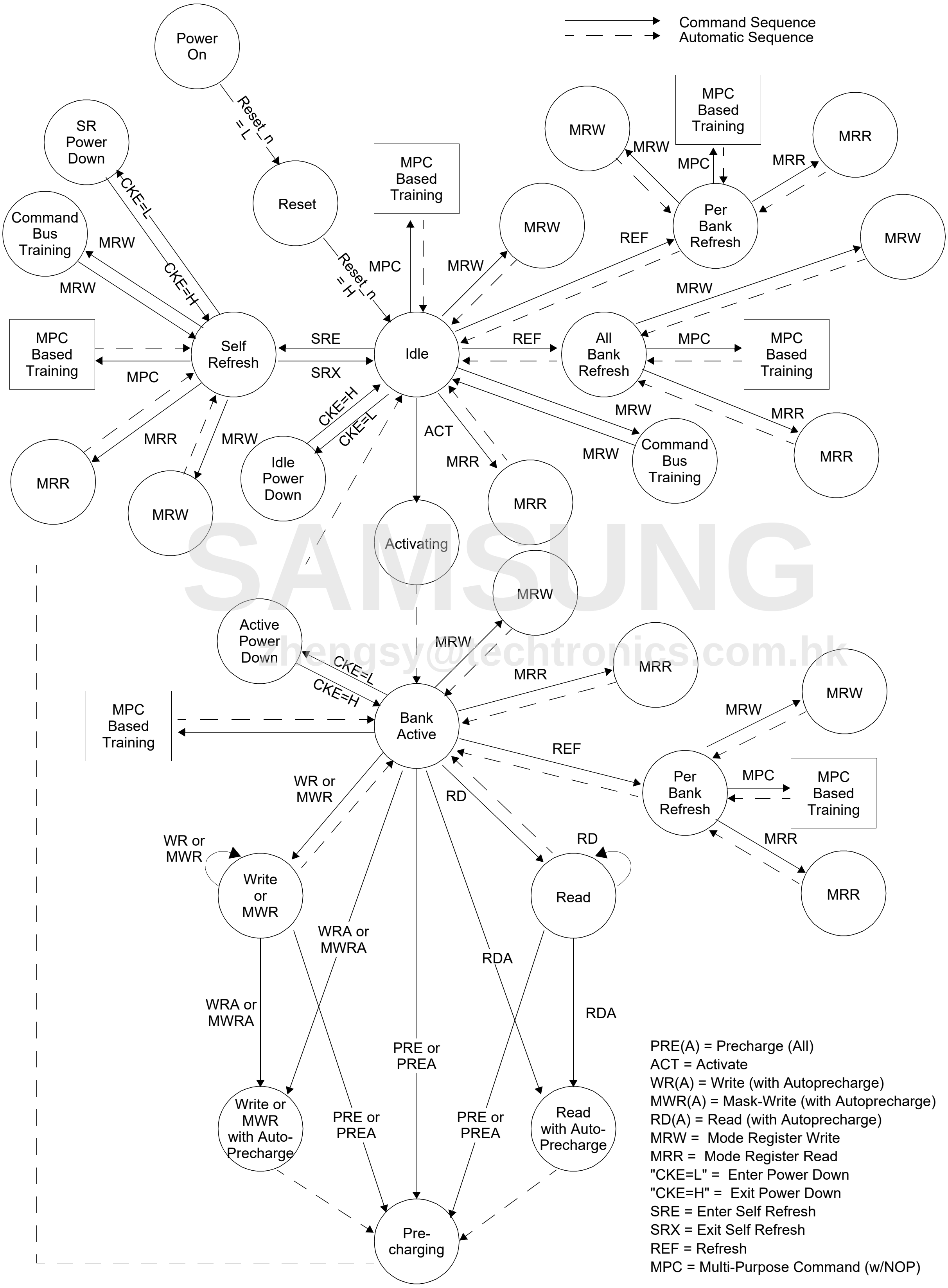
NOTE :
1) The lower two column addresses (C0-C1) are assumed to be “zero” and are not transmitted on the CA bus.
2) Row and Column Address values on the CA bus that are not used for a particular density is required to at valid logic levels.

5.2 Simplified LPDDR4X State Diagram

LPDDR4X-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see datasheet of [Command Definition & Timing Diagram].



PRE(A) = Precharge (All)
ACT = Activate
WR(A) = Write (with Autoprecharge)
MWR(A) = Mask-Write (with Autoprecharge)
RD(A) = Read (with Autoprecharge)
MRW = Mode Register Write
MRR = Mode Register Read
"CKE=L" = Enter Power Down
"CKE=H" = Exit Power Down
SRE = Enter Self Refresh
SRX = Exit Self Refresh
REF = Refresh
MPC = Multi-Purpose Command (w/NOP)

Figure 1. LPDDR4X: Simplified Bus Interface State Diagram-1

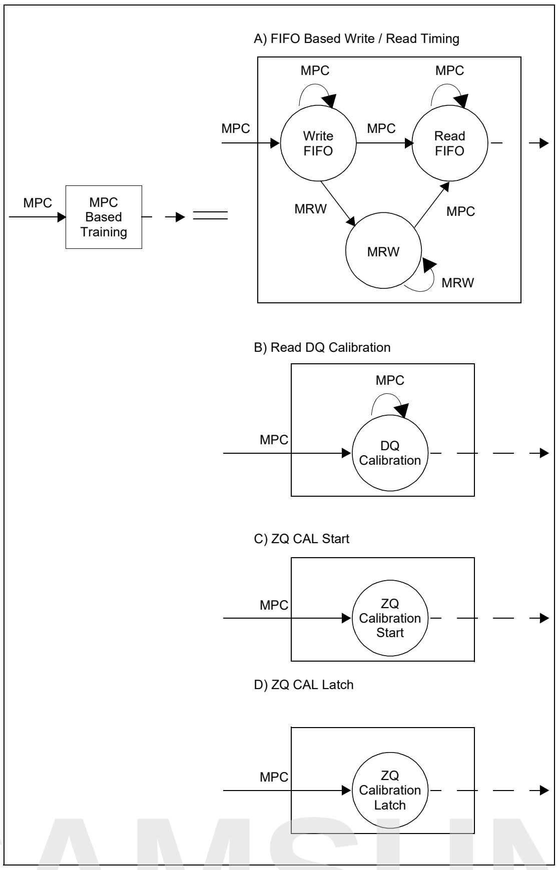


Figure 2. LPDDR4X: Simplified Bus Interface State Diagram -2

NOTE :
1) From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
2) In IDLE state, all banks are precharged.
3) In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
4) In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
5) This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
6) States that have an “automatic return” and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
7) The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

5.3 Mode Register Definition

5.3.1 Mode Register Assignment and Definition in LPDDR4X SDRAM

Table 3 shows the mode registers for LPDDR4X SDRAM. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

[Table 3] Mode Register Assignment in LPDDR4X SDRAM

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info.	R	CATR	(RFU)	Single ended mode	RZQI		(RFU)		Refresh mode
1	01_H	Device Feature 1	W	RPST0	nWR0			RD-PRE0	WR-PRE0	BL	
				RPST1	nWR1			RD-PRE1	WR-PRE1		
2	02_H	Device Feature 2	W	WR Lev	WL Select0	WL0			RL0		
					WL Select1	WL1			RL1		
3	03_H	I/O Configuration-1	W	DBI-WR0	DBI-RD0	PDDS0			PPR Protection	WR PST	PU-CAL0
				DBI-WR1	DBI-RD1	PDDS1				WR PST	PU-CAL1
4	04_H	Refresh Rate	R/W	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
5	05_H	Basic Configuration-1	R	LPDDR4X Manufacturer ID							
6	06_H	Basic Configuration-2	R	Revision ID-1							
7	07_H	Basic Configuration-3	R	Revision ID-2							
8	08_H	Basic Configuration-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor Specific Test Register							
10	$0A_H$	IO Calibration	W	(RFU)							ZQ-RESET
11	$0B_H$	ODT Feature	W	(RFU)	CA ODT0			(RFU)	DQ ODT0		
					CA ODT1				DQ ODT1		
12	$0C_H$	VREF(ca) Setting/Range	R/W	(RFU)	VR-CA0	VREF0(ca)					
					VR-CA1	VREF1(ca)					
13	$0D_H$	CBT,RPT,VRO,VRCG, RRO, DM_DIS,FSP-WR,FSP-OP	W	FSP-OP	FSP-WR	DM_DIS	RRO	VRCG	VRO	RPT	CBT
14	$0E_H$	VREF(dq) Setting/Range	R/W	(RFU)	VR-DQ0	$V_{REF0(DQ)}$					
				(RFU)	VR-DQ1	$V_{REF1(DQ)}$					
15	$0F_H$	Lower-Byte Invert for DQ Calibration	W	Lower-Byte Invert Register for DQ Calibration							
16	10_H	PASR_Bank	W	PASR Bank Mask							
17	11_H	PASR_Segment	W	PASR Segment Mask							
18	12_H	IT-LSB	R	DQS Oscillator Count-LSB							
19	13_H	IT-MSB	R	DQS Oscillator Count-MSB							
20	14_H	Upper-Byte Invert for DQ Calibration	W	Upper-Byte Invert Register for DQ Calibration							
21	15_H	Low Speed CA Buffer	W	(RFU)		Low Speed CA buffer	(RFU)				

[Table 3] Mode Register Assignment in LPDDR4X SDRAM

MR#	MA <7:0>	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
22	16_H	ODT Feature	W	(RFU)		ODT-CA0	ODT-CS0	ODT-CK0	SoC ODT0		
						ODT-CA1	ODT-CS1	ODT-CK1	SoC ODT1		
23	17_H	DQS interval timer run time	W	DQS interval timer run time setting							
24	18_H	TRR	R/W	TRR Mode	TRR Mode BAn			Unlimited MAC	MAC Value		
25	19_H	PPR Resource	R	Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0
26:29	$1A_H$: $1D_H$	RFU	N/A	Reserved for Future Use							
30	$1E_H$	Reserved for Testing	N/A	Reserved for Testing-SDRAM will ignore							
31	$1F_H$	RFU	N/A	Bytemode Vref Selection		Reserved for Future Use					
32	20_H	DQ Calibration Pattern A	W	DQ Calibration Pattern "A" (default = 5AH)							
33:38	21_H~26_H	(Do Not Use)	NA	Do Not Use							
39	27_H	Reserved for Testing	N/A	Reserved for Testing-SDRAM will ignore							
40	28_H	DQ Calibration Pattern B	W	DQ Calibration Pattern "B" (default = 3CH)							
41:47	29_H~$2F_H$	(Do Not Use)	NA	Do Not Use							
48:50	30_H~32_H	RFU	NA	(RFU)							
51	33_H	Single Ended RDQS, WDQS, CLK	W	(RFU)				Single ended Clock	Single ended WDQS	Single ended RDQS	(RFU)
52:63	34_H~$3F_H$	RFU	NA	(RFU)							

🟦	Applied when FSP = 0
🟨	Applied when FSP = 1

NOTE :
1) RFU bits shall be set to ‘0’ during writes.
2) RFU bits shall be read as ‘0’ during reads.
3) All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
4) All mode registers that are specified as RFU shall not be written.
5) Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
CATR	(RFU)	Single ended mode	RZQI		(RFU)		Refresh mode

Function	Register Type	Operand	Data	Notes
Refresh mode	Read-only	OP[0]	0_B: Both legacy & modified refresh mode supported 1_B: Only modified refresh mode supported	
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	**00_B:** RZQ self-test not supported **01_B:** ZQ-pin may connect to V_{SSQ} or float **10_B:** ZQ-pin may short to V_{DDQ} **11_B:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V_{SSQ} or float, nor short to V_{DDQ})	1,2,3,4
Single ended mode		OP[5]	0_B: No support for Single ended mode 1_B: Supports for Single ended mode	6
CATR (CA Terminating Rank)		OP[7]	0_B: CA for this rank is not terminated 1_B: Vendor specific	5

NOTE :

1) RZQI MR value, if supported, will be valid after the following sequence:
   a. Completion of MPC ZQCAL Start command to either channel.
   b. Completion of MPC ZQCAL Latch command to either channel then t_{ZQLAT} is satisfied.
   RZQI value will be lost after Reset.
2) If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01_B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01_B or OP[4:3] =10_B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3) In the case of possible assembly error, the LPDDR4X-SDRAM device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the device may not function as intended.
4) In ZQ self-test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240-Ω +/- 1%).
5) CATR functionality is Vendor specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the vendor device datasheet for details.
6) Support for Single Ended Mode is optional. If supported, Single Ended Write DQS, Read DQS and CK can be enabled in MR51.

MR1_Device Feature 1 (MA<7:0> = 01_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Register Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	**00_B:** BL=16 Sequential (default) **01_B:** BL=32 Sequential **10_B:** BL=16 or 32 Sequential (on-the-fly) **All others:** Reserved	1,7
WR-PRE (WR Pre-amble Length)		OP[2]	**0_B:** Reserved **1_B:** WR Pre-amble = 2×tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	**0_B:** RD Pre-amble = Static (default) **1_B:** RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Precharge commands)		OP[6:4]	**000_B:** nWR = 6 (default) **001_B:** nWR = 10 **010_B:** nWR = 16 **011_B:** nWR = 20 **100_B:** nWR = 24 **101_B:** nWR = 30 **110_B:** nWR = 34 **111_B:** nWR = 40	2,5,6
RPST (RD Post-Amble Length)		OP[7]	**0_B:** RD Post-amble = 0.5×tCK (default) **1_B:** RD Post-amble = 1.5×tCK	4,5,6

NOTE :

1) Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands. See the Command Truth Table.
2) The programmed value of nWR is the number of clock cycles the LPDDR4X-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled. See "Read and Write Latencies" later in this section.
3) For Read operations this bit must be set to select between a “toggling” pre-amble and a “Non-toggling” pre-amble. See the Read Preamble and Postamble section in Operation timing for a drawing of each type of pre-amble.
4) OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be read from with an MRR command to this MR address.
6) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
7) Supporting the two physical registers for Burst Length: MR1 OP[1:0] as optional feature. Applications requiring support of both vendor options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to vendor datasheets for detail.

[Table 4] Read and Write Latencies for x16 mode

Read Latency [nCK]		Write Latency [nCK]		nWR [nCK]	nRTP [nCK]	Lower Clock Frequency Limit [MHz] (Greater than)	Upper Clock Frequency Limit [MHz] (Same or less than)	Notes
No DBI	w/ DBI	Set "A"	Set "B"					
6	6	4	4	6	8	10	266	1,2,3,4,5,6
10	12	6	8	10	8	266	533	
14	16	8	12	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	

NOTE :

1) The LPDDR4X-SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2) DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0_B, then the “No DBI” column should be used for Read Latency. When MR3 OP[6]=1_B, then the “w/DBI” column should be used for Read Latency.
3) Write Latency Set “A” and Set “B” is determined by MR2 OP[6]. When MR2 OP[6]=0_B, then Write Latency Set “A” should be used. When MR2 OP[6]=1_B, then Write Latency Set “B” should be used.
4) The programmed value of nWR is the number of clock cycles the LPDDR4X-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto precharge). It is determined by RU(tWR/tCK).
5) The programmed value of nRTP is the number of clock cycles the LPDDR4X-SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (auto precharge). It is determined by RU(tRTP/tCK).
6) nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

[Table 5] Burst Sequence for READ

BL	BT	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	seq	V	0_B	0_B	0_B	0_B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
		V	0_B	1_B	0_B	0_B	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																
		V	1_B	0_B	0_B	0_B	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																
		V	1_B	1_B	0_B	0_B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																
32	seq	0_B	0_B	0_B	0_B	0_B	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0_B	0_B	1_B	0_B	0_B	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0_B	1_B	0_B	0_B	0_B	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0_B	1_B	1_B	0_B	0_B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1_B	0_B	0_B	0_B	0_B	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1_B	0_B	1_B	0_B	0_B	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1_B	1_B	0_B	0_B	0_B	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1_B	1_B	1_B	0_B	0_B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

NOTE :
1) C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2) The starting burst address is on 64-bit (4n) boundaries.

[Table 6] Burst Sequence for Write

BL	BT	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	seq	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																
32	seq	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

NOTE :
1) C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2) The starting address is on 256-bit (16n) boundaries for Burst length 16.
3) The starting address is on 512-bit (32n) boundaries for Burst length 32.
4) C2-C3 shall be set to '0' for all Write operations.

MR2_Device Feature 2 (MA<7:0> = 02$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
WR Lev	WLS	WL			RL		

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write-only	OP[2:0]	**RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0$_B$)** **000**$_B$: RL=6, nRTP=8 (Default) **001**$_B$: RL=10, nRTP=8 **010**$_B$: RL=14, nRTP=8 **011**$_B$: RL=20, nRTP=8 **100**$_B$: RL=24, nRTP=10 **101**$_B$: RL=28, nRTP=12 **110**$_B$: RL=32, nRTP=14 **111**$_B$: RL=36, nRTP=16 **RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1$_B$)** **000**$_B$: RL= 6, nRTP=8 **001**$_B$: RL= 12, nRTP=8 **010**$_B$: RL= 16, nRTP=8 **011**$_B$: RL= 22, nRTP=8 **100**$_B$: RL= 28, nRTP=10 **101**$_B$: RL= 32, nRTP=12 **110**$_B$: RL= 36, nRTP=14 **111**$_B$: RL= 40, nRTP=16	1,3,4
WL (Write latency)		OP[5:3]	**WL Set "A" (MR2 OP[6]=0$_B$)** **000**$_B$: WL=4 (Default) **001**$_B$: WL=6 **010**$_B$: WL=8 **011**$_B$: WL=10 **100**$_B$: WL=12 **101**$_B$: WL=14 **110**$_B$: WL=16 **111**$_B$: WL=18 **WL Set "B" (MR2 OP[6]=1$_B$)** **000**$_B$: WL=4 **001**$_B$: WL=8 **010**$_B$: WL=12 **011**$_B$: WL=18 **100**$_B$: WL=22 **101**$_B$: WL=26 **110**$_B$: WL=30 **111**$_B$: WL=34	1,3,4
WLS (Write latency set)		OP[6]	**0**$_B$: WL Set "A" (default) **1**$_B$: WL Set "B"	1,3,4
WR Leveling		OP[7]	**0**$_B$: Disabled (default) **1**$_B$: Enabled	2

NOTE :
1) See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP.
2) After a MRW to set the Write Leveling Enable bit (OP[7]=1$_B$), the LPDDR4X-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0$_B$). No other commands are allowed until the Write Leveling Enable bit is cleared.
3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
4) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR3_I/O Configuration 1 (MA<7:0> = 03$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-Cal (Pull-up Calibration Point)	Write-only	OP[0]	**0$_B$**: V_{DDQ}×0.6 **1$_B$**: V_{DDQ}×0.5 (default)	1,4
WR PST (WR Post-Amble Length)		OP[1]	**0$_B$**: WR Post-amble = 0.5×tCK (default) **1$_B$**: WR Post-amble = 1.5×tCK (Vendor specific function)	2,3,5
Post Package Repair Protection		OP[2]	**0$_B$**: PPR protection disabled (default) **1$_B$**: PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	**000$_B$**: RFU **001$_B$**: RZQ/1 **010$_B$**: RZQ/2 **011$_B$**: RZQ/3 **100$_B$**: RZQ/4 **101$_B$**: RZQ/5 **110$_B$**: RZQ/6 (default) **111$_B$**: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	**0$_B$**: Disabled (default) **1$_B$**: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	**0$_B$**: Disabled (default) **1$_B$**: Enabled	2,3

NOTE :

1) All values are “typical”. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4) For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5) Refer to the supplier data sheet for vender specific function. 1.5×tCK apply > 1.6GHz clock.
6) If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

MR4_Refresh rate (MA<7:0> = 04_H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read-only	OP[2:0]	**000**$_B$: SDRAM Low temperature operating limit exceeded **001**$_B$: 4x refresh **010**$_B$: 2x refresh **011**$_B$: 1x refresh (default) **100**$_B$: 0.5x refresh **101**$_B$: 0.25x refresh, no de-rating **110**$_B$: 0.25x refresh, with de-rating **111**$_B$: SDRAM High temperature operating limit exceeded	1,2,3,4 7,8,9
SR Abort (Self Refresh Abort)	Write-only	OP[3]	**0**$_B$: Disable (default) **1**$_B$: Enable	9,11
PPRE (Post-package repair entry/exit)	Write-only	OP[4]	**0**$_B$: Exit PPR mode (default) **1**$_B$: Enter PPR mode	5,9
Thermal Offset (Vender Specific Function)	Write-only	OP[6:5]	**00**$_B$: No offset, 0~5°C gradient (default) **01**$_B$: 5°C offset, 5~10°C gradient **10**$_B$: 10°C offset, 10~15°C gradient **11**$_B$: Reserved	10
TUF (Temperature Update Flag)	Read-only	OP[7]	**0**$_B$: No change in OP[2:0] since last MR4 read (default) **1**$_B$: Change in OP[2:0] since last MR4 read	6,7,8

NOTE :
1) The refresh rate for each MR4 OP[2:0] setting applies to tREFI, tREFIpb and tREFW. OP[2:0]=011_B corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1_B, the device temperature is greater than 85°C.
2) At higher temperatures (>85°C), AC timing derating may be required. If derating is required the LPDDR4X-SDRAM will set OP[2:0]=110_B. See derating timing requirements in the AC Timing section.
3) DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4) The device may not operate properly when OP[2:0]=000_B or 111_B.
5) Post-package repair can be entered or exited by writing to OP[4].
6) When OP[7]=1_B, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to ‘0’.
7) OP[7]=0_B at power-up. OP[2:0] bits are valid after initialization sequence (Te).
8) See the section on “Temperature Sensor” for information on the recommended frequency of reading MR4.
9) OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
10) Refer to the supplier data sheet for vender specific function.
11) Self refresh abort feature is available for higher density devices starting with 12Gb device.

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR4X Manufacturer ID							

Function	Register Type	Operand	Data	Notes
LPDDR4X Manufacturer ID	Read-only	OP[7:0]	**0000 0001**$_B$: Samsung	

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID-1							

Function	Register Type	Operand	Data	Notes
LPDDR4X Revision ID-1	Read-only	OP[7:0]	**0000 1000**$_B$: I-version	1

NOTE :
1) MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID-2							

Function	Register Type	Operand	Data	Notes
LPDDR4X Revision ID-2	Read-only	OP[7:0]	**$0000\ 0000_B$**	1

NOTE :
1) MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = 08_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Function	Register Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	**00_B:** LPDDR4 S16 SDRAM (16n pre-fetch) Standard VDDQ(1.1V) only **10_B:** LPDDR4X S16 SDRAM (16n pre-fetch) LOW VDDQ(0.6V) support only **All Others**: Reserved	
Density		OP[5:2]	**0000_B**: 4Gb dual channel die / 2Gb single channel die **0001_B**: 6Gb dual channel die / 3Gb single channel die **0010_B**: 8Gb dual channel die / 4Gb single channel die **0011_B**: 12Gb dual channel die / 6Gb single channel die **0100_B**: 16Gb dual channel die / 8Gb single channel die **0101_B**: 24Gb dual channel die / 12Gb single channel die **0110_B**: 32Gb dual channel die / 16Gb single channel die **All Others**: Reserved	
I/O width		OP[7:6]	**00_B**: x16 (per channel) **All Others** : Reserved	

MR9_Test Mode (MA<7:0> = 09_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Register							

NOTE :
1) Only 00_H should be written to this register.

MR10_IO Calibration (MA<7:0> = $0A_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)							ZQ-Reset

Function	Register Type	Operand	Data	Notes
ZQ-Reset	Write-only	OP[0]	**0_B**: Normal Operation (Default) **1_B**: ZQ Reset	1,2

NOTE :
1) See ZQCal Timing Parameters for calibration latency and timing in AC Timing table.
2) If the ZQ-pin is connected to V_{DDQ} through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

MR11_ODT Feature (MA<7:0> = $0B_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)	CA ODT			(RFU)	DQ ODT		

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	**000**$_B$: Disable (Default) **001**$_B$: RZQ/1 **010**$_B$: RZQ/2 **011**$_B$: RZQ/3 **100**$_B$: RZQ/4 **101**$_B$: RZQ/5 **110**$_B$: RZQ/6 **111**$_B$: RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)		OP[6:4]	**000**$_B$: Disable (Default) **001**$_B$: RZQ/1 **010**$_B$: RZQ/2 **011**$_B$: RZQ/3 **100**$_B$: RZQ/4 **101**$_B$: RZQ/5 **110**$_B$: RZQ/6 **111**$_B$: RFU	1,2,3

NOTE :

1) All values are “typical”. The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR12_$V_{REF(CA)}$ Setting/Range (MA<7:0> = $0C_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)	VR-CA	$V_{REF(CA)}$					

Function	Register Type	Operand	Data	Notes
$V_{REF(CA)}$ ($V_{REF(CA)}$ Setting)	Read/Write	OP[5:0]	**000000_B**: -- Thru . **110010_B**: See table below **All Others**: Reserved	1,2,3,5, 6
VR-CA ($V_{REF(CA)}$ Range)		OP[6]	**0_B**: $V_{REF(CA)}$ Range[0] enabled **1_B**: $V_{REF(CA)}$ Range[1] enabled (default)	1,2,4,5, 6

NOTE :

1) This register controls the $V_{REF(CA)}$ levels. Refer to Table 12, VREF Settings for Range[0] and Range[1].
2) A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3) A write to OP[5:0] sets the internal $V_{REF(CA)}$ level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for $V_{REF(CA)}$ to reach the set level depends on the step size from the current level to the new level. See the section on $V_{REF(CA)}$ training for more information.
4) A write to OP[6] switches the LPDDR4X-SDRAM between two internal $V_{REF(CA)}$ ranges. The range (Range[0] or Range[1]) must be selected when setting the $V_{REF(CA)}$ register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

[Table 7] V_{REF} Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (%of V_{DDQ})		Range[1] Values (%of V_{DDQ})		Notes
V_{REF} Settings for MR12	OP[5:0]	**000000_B**: 15.0%	**011010_B**: 30.5%	**000000_B**: 32.9%	**011010_B**: 48.5%	1,2,3
		000001_B: 15.6%	**011011_B**: 31.1%	**000001_B**: 33.5%	**011011_B**: 49.1%	
		000010_B: 16.2%	**011100_B**: 31.7%	**000010_B**: 34.1%	**011100_B**: 49.7%	
		000011_B: 16.8%	**011101_B**: 32.3%	**000011_B**: 34.7%	**011101_B**: 50.3% (Default)	
		000100_B: 17.4%	**011110_B**: 32.9%	**000100_B**: 35.3%	**011110_B**: 50.9%	
		000101_B: 18.0%	**011111_B**: 33.5%	**000101_B**: 35.9%	**011111_B**: 51.5%	
		000110_B: 18.6%	**100000_B**: 34.1%	**000110_B**: 36.5%	**100000_B**: 52.1%	
		000111_B: 19.2%	**100001_B**: 34.7%	**000111_B**: 37.1%	**100001_B**: 52.7%	
		001000_B: 19.8%	**100010_B**: 35.3%	**001000_B**: 37.7%	**100010_B**: 53.3%	
		001001_B: 20.4%	**100011_B**: 35.9%	**001001_B**: 38.3%	**100011_B**: 53.9%	
		001010_B: 21.0%	**100100_B**: 36.5%	**001010_B**: 38.9%	**100100_B**: 54.5%	
		001011_B: 21.6%	**100101_B**: 37.1%	**001011_B**: 39.5%	**100101_B**: 55.1%	
		001100_B: 22.2%	**100110_B**: 37.7%	**001100_B**: 40.1%	**100110_B**: 55.7%	
		001101_B: 22.8%	**100111_B**: 38.3%	**001101_B**: 40.7%	**100111_B**: 56.3%	
		001110_B: 23.4%	**101000_B**: 38.9%	**001110_B**: 41.3%	**101000_B**: 56.9%	
		001111_B: 24.0%	**101001_B**: 39.5%	**001111_B**: 41.9%	**101001_B**: 57.5%	
		010000_B: 24.6%	**101010_B**: 40.1%	**010000_B**: 42.5%	**101010_B**: 58.1%	
		010001_B: 25.1%	**101011_B**: 40.7%	**010001_B**: 43.1%	**101011_B**: 58.7%	
		010010_B: 25.7%	**101100_B**: 41.3%	**010010_B**: 43.7%	**101100_B**: 59.3%	
		010011_B: 26.3%	**101101_B**: 41.9%	**010011_B**: 44.3%	**101101_B**: 59.9%	
		010100_B: 26.9%	**101110_B**: 42.5%	**010100_B**: 44.9%	**101110_B**: 60.5%	
		010101_B: 27.5%	**101111_B**: 43.1%	**010101_B**: 45.5%	**101111_B**: 61.1%	
		010110_B: 28.1%	**110000_B**: 43.7%	**010110_B**: 46.1%	**110000_B**: 61.7%	
		010111_B: 28.7%	**110001_B**: 44.3%	**010111_B**: 46.7%	**110001_B**: 62.3%	
		011000_B: 29.3%	**110010_B**: 44.9%	**011000_B**: 47.3%	**110010_B**: 62.9%	
		011001_B: 29.9%	**All Others**: Reserved	**011001_B**: 47.9%	**All Others**: Reserved	

NOTE:

1) These values may be used for MR12 OP[5:0] to set the $V_{REF(CA)}$ levels in the LPDDR4X-SDRAM.
2) The range may be selected in the MR12 register by setting OP[6] appropriately.
3) The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

MR13_CBT,RPT,VRO,VRCG,RRO,DM_DIS,FSP-WR, FSP-OP (MA<7:0> = $0D_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write-only	OP[0]	**0_B**: Normal Operation (default) **1_B**: Command Bus Training Mode Enabled	1
RPT (Read Preamble Training Mode)		OP[1]	**0_B**: Disable (default) **1_B**: Enable	
VRO (V_{REF} Output)		OP[2]	**0_B**: Normal operation (default) **1_B**: Output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ values on DQ bits	2
VRCG (V_{REF} Current Generator)		OP[3]	**0_B**: Normal operation (default) **1_B**: V_{REF} fast response (high current) mode	3
RRO (Refresh Rate Option)		OP[4]	**0_B**: Disable codes 001 and 010 in MR4 OP[2:0] **1_B**: Enable all codes in MR4 OP[2:0]	4,5
DMD (Data Mask Disable)		OP[5]	**0_B**: Data Mask Operation Enabled (default) **1_B**: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write/Read)		OP[6]	**0_B**: Frequency-Set-Point [0] (default) **1_B**: Frequency-Set-Point [1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	**0_B**: Frequency-Set-Point [0] (default) **1_B**: Frequency-Set-Point [1]	8

NOTE :

1) A write to set OP[0]=1_B causes the LPDDR4X-SDRAM to enter the Command Bus training mode. When OP[0]=1_B and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0_B) and return to normal operation. See the Command Bus Training section for more information.
2) When set, the LPDDR4X-SDRAM will output the $V_{REF(CA)}$ and $V_{REF(DQ)}$ voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels. The DQ pins used for V_{REF} output are vendor specific.
3) When OP[3]=1_B, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.
4) MR13 OP[4] RRO bit is valid only when MR0 OP[0]= 1_B. For LPDDR4X devices with MR0 OP[0] = 0_B, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5) When OP[4] = 0_B, only 001_B and 010_B in MR4 OP[2:0] are disabled. LPDDR4X devices must report 011_B instead of 001_B or 010_B in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6) When enabled (OP[5]=0_B) data masking is enabled for the device. When disabled (OP[5]=1_B), masked write command is illegal. See LPDDR4X Data Mask (DM) and Data Bus Inversion (DBIdc) Function in operation timing datasheet.
7) FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as $V_{REF(CA)}$ Setting, $V_{REF(CA)}$ Range, $V_{REF(DQ)}$ Setting, $V_{REF(DQ)}$ Range. For more information, refer to Frequency Set Point section in operations and timing spec.
8) FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as $V_{REF(CA)}$ Setting, $V_{REF(CA)}$ Range, $V_{REF(DQ)}$ Setting, $V_{REF(DQ)}$ Range. For more information, refer to Frequency Set Point section in operations and timing spec.

MR14_$V_{REF(DQ)}$ Setting/Range (MA<7:0> = $0E_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)	VR(DQ)	$V_{REF(DQ)}$					

Function	Register Type	Operand	Data	Notes
$V_{REF(DQ)}$ ($V_{REF(DQ)}$ Setting)	Read/Write	OP[5:0]	$\mathbf{000000}_B$: -- Thru . $\mathbf{110010}_B$: See table below **All Others**: Reserved	1,2,3,5,6
$V_{REF(DQ)}$ ($V_{REF(DQ)}$ Range)		OP[6]	$\mathbf{0}_B$: $V_{REF(DQ)}$ Range [0] enabled $\mathbf{1}_B$: $V_{REF(DQ)}$ Range [1] enabled (default)	1,2,4,5,6

NOTE :

1) This register controls the $V_{REF(DQ)}$ levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(DQ)[1] may be selected by setting OP[6] appropriately.
2) A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3) A write to OP[5:0] sets the internal $V_{REF(DQ)}$ level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for $V_{REF(DQ)}$ to reach the set level depends on the step size from the current level to the new level. See the section on $V_{REF(DQ)}$ training for more information.
4) A write to OP[6] switches the LPDDR4X-SDRAM between two internal $V_{REF(DQ)}$ ranges. The range (Range[0] or Range[1]) must be selected when setting the $V_{REF(DQ)}$ register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

[Table 8] VREF Settings for Range[0] and Range[1]

Function	Operand	Range[0] Values (%of VDDQ)		Range[1] Values (%of VDDQ)		Notes
VREF Settings for MR14	OP[5:0]	$\mathbf{000000}_B$: 15.0%	$\mathbf{011010}_B$: 30.5%	$\mathbf{000000}_B$: 32.9%	$\mathbf{011010}_B$: 48.5%	1,2,3
		$\mathbf{000001}_B$: 15.6%	$\mathbf{011011}_B$: 31.1%	$\mathbf{000001}_B$: 33.5%	$\mathbf{011011}_B$: 49.1%	
		$\mathbf{000010}_B$: 16.2%	$\mathbf{011100}_B$: 31.7%	$\mathbf{000010}_B$: 34.1%	$\mathbf{011100}_B$: 49.7%	
		$\mathbf{000011}_B$: 16.8%	$\mathbf{011101}_B$: 32.3%	$\mathbf{000011}_B$: 34.7%	$\mathbf{011101}_B$: 50.3% (Default)	
		$\mathbf{000100}_B$: 17.4%	$\mathbf{011110}_B$: 32.9%	$\mathbf{000100}_B$: 35.3%	$\mathbf{011110}_B$: 50.9%	
		$\mathbf{000101}_B$: 18.0%	$\mathbf{011111}_B$: 33.5%	$\mathbf{000101}_B$: 35.9%	$\mathbf{011111}_B$: 51.5%	
		$\mathbf{000110}_B$: 18.6%	$\mathbf{100000}_B$: 34.1%	$\mathbf{000110}_B$: 36.5%	$\mathbf{100000}_B$: 52.1%	
		$\mathbf{000111}_B$: 19.2%	$\mathbf{100001}_B$: 34.7%	$\mathbf{000111}_B$: 37.1%	$\mathbf{100001}_B$: 52.7%	
		$\mathbf{001000}_B$: 19.8%	$\mathbf{100010}_B$: 35.3%	$\mathbf{001000}_B$: 37.7%	$\mathbf{100010}_B$: 53.3%	
		$\mathbf{001001}_B$: 20.4%	$\mathbf{100011}_B$: 35.9%	$\mathbf{001001}_B$: 38.3%	$\mathbf{100011}_B$: 53.9%	
		$\mathbf{001010}_B$: 21.0%	$\mathbf{100100}_B$: 36.5%	$\mathbf{001010}_B$: 38.9%	$\mathbf{100100}_B$: 54.5%	
		$\mathbf{001011}_B$: 21.6%	$\mathbf{100101}_B$: 37.1%	$\mathbf{001011}_B$: 39.5%	$\mathbf{100101}_B$: 55.1%	
		$\mathbf{001100}_B$: 22.2%	$\mathbf{100110}_B$: 37.7%	$\mathbf{001100}_B$: 40.1%	$\mathbf{100110}_B$: 55.7%	
		$\mathbf{001101}_B$: 22.8%	$\mathbf{100111}_B$: 38.3%	$\mathbf{001101}_B$: 40.7%	$\mathbf{100111}_B$: 56.3%	
		$\mathbf{001110}_B$: 23.4%	$\mathbf{101000}_B$: 38.9%	$\mathbf{001110}_B$: 41.3%	$\mathbf{101000}_B$: 56.9%	
		$\mathbf{001111}_B$: 24.0%	$\mathbf{101001}_B$: 39.5%	$\mathbf{001111}_B$: 41.9%	$\mathbf{101001}_B$: 57.5%	
		$\mathbf{010000}_B$: 24.6%	$\mathbf{101010}_B$: 40.1%	$\mathbf{010000}_B$: 42.5%	$\mathbf{101010}_B$: 58.1%	
		$\mathbf{010001}_B$: 25.1%	$\mathbf{101011}_B$: 40.7%	$\mathbf{010001}_B$: 43.1%	$\mathbf{101011}_B$: 58.7%	
		$\mathbf{010010}_B$: 25.7%	$\mathbf{101100}_B$: 41.3%	$\mathbf{010010}_B$: 43.7%	$\mathbf{101100}_B$: 59.3%	
		$\mathbf{010011}_B$: 26.3%	$\mathbf{101101}_B$: 41.9%	$\mathbf{010011}_B$: 44.3%	$\mathbf{101101}_B$: 59.9%	
		$\mathbf{010100}_B$: 26.9%	$\mathbf{101110}_B$: 42.5%	$\mathbf{010100}_B$: 44.9%	$\mathbf{101110}_B$: 60.5%	
		$\mathbf{010101}_B$: 27.5%	$\mathbf{101111}_B$: 43.1%	$\mathbf{010101}_B$: 45.5%	$\mathbf{101111}_B$: 61.1%	
		$\mathbf{010110}_B$: 28.1%	$\mathbf{110000}_B$: 43.7%	$\mathbf{010110}_B$: 46.1%	$\mathbf{110000}_B$: 61.7%	
		$\mathbf{010111}_B$: 28.7%	$\mathbf{110001}_B$: 44.3%	$\mathbf{010111}_B$: 46.7%	$\mathbf{110001}_B$: 62.3%	
		$\mathbf{011000}_B$: 29.3%	$\mathbf{110010}_B$: 44.9%	$\mathbf{011000}_B$: 47.3%	$\mathbf{110010}_B$: 62.9%	
		$\mathbf{011001}_B$: 29.9%	**All Others**: Reserved	$\mathbf{011001}_B$: 47.9%	**All Others**: Reserved	

NOTE:

1) These values may be used for MR14 OP[5:0] to set the $V_{REF(DQ)}$ levels in the LPDDR4X-SDRAM.
2) The range may be selected in the MR14 register by setting OP[6] appropriately.
3) The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

MR15_Lower-Byte Invert for DQ Calibration (MA<7:0> = 0F$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Lower-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: **0$_B$**: Do not invert **1$_B$**: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55$_H$	1,2,3

NOTE :
1) This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101$_B$, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2) DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3) No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

[Table 9] MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR16_PASR_Bank Mask (MA<7:0> = 010$_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Bank Mask							

Function	Register Type	Operand	Data	Notes
Bank [7:0] Mask	Write-only	OP[7:0]	**0$_B$:** Bank Refresh Enabled (default) : Unmasked **1$_B$:** Bank Refresh disabled : Masked	1

OP	Bank Mask	8-Bank SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

NOTE :
1) When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2) PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

MR17_PASR Segment Mask (MA<7:0> = 011_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write-only	OP[7:0]	**0_B:** Segment Refresh enabled (default) **1_B:** Segment Refresh disabled	

Segment	OP	Segment Mask	2Gb per channel	3Gb per channel	4Gb per channel	6Gb per channel	8Gb per channel	12Gb per channel	16Gb per channel
			R13:11	R14:12	R14:12	R15:13	R15:13	R16:14	R16:14
0	0	XXXXXXX1	**000_B**						
1	1	XXXXXX1X	**001_B**						
2	2	XXXXX1XX	**010_B**						
3	3	XXXX1XXX	**011_B**						
4	4	XXX1XXXX	**100_B**						
5	5	XX1XXXXX	**101_B**						
6	6	X1XXXXXX	**110_B**	**Not Allowed**	**110_B**	**Not Allowed**	**110_B**	**Not Allowed**	**110_B**
7	7	1XXXXXXX	**111_B**		**111_B**		**111_B**		**111_B**

NOTE :

1) This table indicates the range of row addresses in each masked segment. "X" is don’t care for a particular segment.
2) PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.
3) For 3Gb, 6Gb and 12Gb per channel densities, OP[7:6] must always be LOW (=00B).

MR18_IT-LSB (MA<7:0> = 12_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count-LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 LSB DRAM DQS Oscillator Count	1,2,3

NOTE :

1) MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2) Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3) A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR19_IT-MSB (MA<7:0> = 13_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS Oscillator Count-MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

NOTE :

1) MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2) Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3) A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR20_Upper-Byte Invert for DQ Calibration (MA<7:0> = 14_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Upper-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55_H	1,2

NOTE:

1) This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2) DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3) No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

[Table 10] MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR21_Low Speed CA Buffer (MA<7:0> = 015_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)		Low Speed CA buffer	(RFU)				

Function	Register Type	Operand	Data	Notes
Low Speed CA Buffer	Write-only	OP[5]	0_B: Normal CA Buffer (Default) 1_B:Low Speed CA Buffer	1,2,3,4,5,6,7

NOTE :

1) Support for the Low Speed CA Buffer feature enabled by MR21 OP[5] is optional. Refer to manufacturer data sheet for availability.
2) Low Speed CA Buffer feature can enable lower power for some manufacturers' designs. The maximum clock speed for this mode is vendor-specific, but is not above 800 MHz. Refer to manufacturer data sheet for details.
3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
5) After completing all the other MRW commands to set the values besides MR21 OP[5] setting, MR21 OP[5] can be enabled to "High". Low Power CA Buffer cannot be enabled prior to full device initialization (completion of Step 9 in power up sequence).
6) Low speed CA buffer is allowed to be enabled only when CA ODT is disabled.
7) SDRAM not supporting Low Speed CA Buffer will ignore MR21 OP[5] setting.

MR22_ODT Feature (MA<7:0> = 16_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)		ODT-CA	ODT-CS	ODT-CK	SoC ODT		

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	**000_B**: Disable (Default) **001_B**: RZQ/1 (illegal if MR3 OP0=0_B) **010_B**: RZQ/2 **011_B**: RZQ/3 (illegal if MR3 OP0=0_B) **100_B**: RZQ/4 **101_B**: RZQ/5 (illegal if MR3 OP0=0_B) **110_B**: RZQ/6 (illegal if MR3 OP0=0_B) **111_B**: RFU	1,2,3
ODT-CK		OP[3]	ODT bond PAD is ignored **0_B** : ODT-CK Enable (Default) **1_B** : ODT-CK Disable	2,3,4
ODT-CS		OP[4]	ODT bond PAD is ignored **0_B**: ODT-CS Enable (Default) **1_B**: ODT-CS Disable	2,3,4
ODT-CA		OP[5]	ODT bond PAD is ignored **0_B**: ODT-CA Enable (default) **1_B**: ODT-CA Disabled	2,3,4

NOTE :
1) All values are “typical”.
2) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4) LPDDR4X device ignore ODT bond PAD.

[Table 11] DRAM PU strength & SoC ODT relation

VOH CAL (MR3 OP0)		SoC ODT Value (MR22 OP[2:0])							
		000_B	001_B	010_B	011_B	100_B	101_B	110_B	111_B
0_B (VOH=VDDQ*3/5)	SoC ODT	Disable	illegal	RZQ/ 2=120ohm	illegal	RZQ/ 4=60ohm	illegal	illegal	RFU
	DRAM Pull-up	Default	N/A	RZQ/ 3=80ohm	N/A	RZQ/ 6=40ohm	N/A	N/A	RFU
1_B (VOH=VDDQ/2)	SoC ODT	Disable	RZQ/ 1=240ohm	RZQ/ 2=120ohm	RZQ/ 3=80ohm	RZQ/ 4=60ohm	RZQ/ 5=48ohm	RZQ/ 6=40ohm	RFU
	DRAM Pull-up	Default	RZQ/ 1=240ohm	RZQ/ 2=120ohm	RZQ/ 3=80ohm	RZQ/ 4=60ohm	RZQ/ 5=48ohm	RZQ/ 6=40ohm	RFU

A) There is no corresponding RZQ/x value for 001B,011B,101B,110B when MR3 OP0 = 0B to support 3/5 VDDQ VOH value.

MR23_DQS Interval Timer Run Time (MA<7:0> = 17_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQS interval timer run time setting							

Function	Register Type	Operand	Data	Notes
DQS interval timer run time	Write-only	OP[7:0]	**00000000**$_B$: DQS interval timer stop via MPC Command **(Default)** **00000001**$_B$: DQS timer stops automatically at 16th clocks after timer start **00000010**$_B$: DQS timer stops automatically at 32nd clocks after timer start **00000011**$_B$: DQS timer stops automatically at 48th clocks after timer start **00000100**$_B$: DQS timer stops automatically at 64th clocks after timer start -------------- Thru ---------------------- **00111111**$_B$: DQS timer stops automatically at (63X16)th clocks after timer start **01XXXXXX**$_B$: DQS timer stops automatically at 2048th clocks after timer start **10XXXXXX**$_B$: DQS timer stops automatically at 4096th clocks after timer start **11XXXXXX**$_B$: DQS timer stops automatically at 8192nd clocks after timer start	1,2

NOTE :
1) MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000_B.
2) MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

MR24_TRR (MA<7:0> = 18_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TRR Mode	TRR mode BAn			Unlimited MAC	MAC Value		

Function	Register Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	**000**$_B$: Unknown when bit OP3 =0 1) Unlimited when bit OP3=1 2) **001**$_B$: 700K **010**$_B$: 600K **011**$_B$: 500K **100**$_B$: 400K **101**$_B$: 300K **110**$_B$: 200K **111**$_B$: Reserved	
Unlimited MAC		OP[3]	**0**$_B$: OP[2:0] define MAC value **1**$_B$: Unlimited MAC value 2), 3)	
TRR Mode BAn	Write-only	OP[6:4]	**000**$_B$: Bank 0 **001**$_B$: Bank 1 **010**$_B$: Bank 2 **011**$_B$: Bank 3 **100**$_B$: Bank 4 **101**$_B$: Bank 5 **110**$_B$: Bank 6 **111**$_B$: Bank 7	
TRR Mode		OP[7]	**0**$_B$: Disabled (default) **1**$_B$: Enabled	

NOTE :
1) Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2) There is no restriction to number of activates.
3) MR24 OP [2:0] is set to ZERO.

MR25_PPR Resources (MA<7:0> = 19_H):

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank 7	Bank 6	Bank 5	Bank 4	Bank 3	Bank 2	Bank 1	Bank 0

Function	Register Type	Operand	Data	Notes
PPR Resource	Read-only	OP[7:0]	0_B: PPR Resource is not available 1_B: PPR Resource is available	

MR26-29_(RFU) (MA<7:0> = $1A_H$ - $1D_H$):

MR30_Reserved for Testing (MA<7:0> = $1E_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Register Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

NOTE :
1) This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR31_Bytemode Vref Selection (MA<7:0> = $1F_H$):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bytemode Vref Selection		(RFU)					

Function	Register Type	Operand	Data	Notes
Bytemode Vref Selection Lower Byte	Write-only	OP[6]	0_B: x16 device and no Byte mode selection (Default) 1_B: Disable to update MR12/MR14 for lower byte	1,2,3
Bytemode Vref Selection Upper Byte		OP[7]	0_B: x16 device and no Byte mode selection (Default) 1_B: Disable to update MR12/MR14 for upper byte	1,2,3

NOTE :
1) The byte mode Vref selection is optional. Please consult with vendors for the availability to support feature.
2) When Byte mode Vref selection is applied, the non-targeted byte is required to disable to update VrefCA and VrefDQ setting, assigned in MR12 and MR14 OP[6:0], for the other targeted byte.
   - In order to update MR12/MR14 setting only for upper byte, it is required to disable byte mode selection on lower byte, as applying MR31 OP[7:6] = 01B.
   - In order to update MR12/MR14 setting only for lower byte, it is required to disable byte mode selection on upper byte, as applying MR31 OP[7:6] = 10B.
   - When OP[7:6] = 00B is applied, both lower byte and upper byte will be updated.
3) When the configuration is not composed of byte mode device, MR31 OP[7:6] shall be the default value, 00B.

MR32_DQ Calibration Pattern A (MA<7:0>=20_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern "A" (default = $5A_H$)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	X_B: An MPC command with OP[6:0]=1000011_B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "$5A_H$" is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	

MR33:38_(Do Not Use) (MA<7:0> = 21_H-26_H):

MR39_Reserved for Testing (MA<7:0> = 27_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Valid 0 or 1							

Function	Register Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don’t care	1

NOTE :

1) This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
DQ Calibration Pattern “B” (default = $3C_H$)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write-only	OP[7:0]	**X_B**: A default pattern “$3C_H$” is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32,for more information.	1,2,3

NOTE :

1) The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized “little endian” such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H, then the first bit transmitted with be a ‘1’, followed by ‘1’, ‘1’, ‘0’, ‘0’, ‘1’, ‘0’, and ‘0’. The bit stream will be 00100111_B.

2) MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.

3) The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].

4) No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3 OP[6].

MR41:47_ (Do Not Use)(MA<7:0> = 29_H-$2F_H$):

MR48:50_(RFU) (MA<7:0> = 30_H - 32_H) :

MR51_Single Ended RDQS, WDQS, Clock (MA<7:0> = 33_H) :

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				Single ended Clock	Single ended WDQS	Single ended RDQS	(RFU)

Function	Register Type	Operand	Data	Notes
Single ended RDQS	Write-only	OP[1]	0_B: Differential Read DQS (Default) 1_B: Single ended Read DQS	1,2,3,4,5
Single ended WDQS		OP[2]	0_B: Differential Write DQS (Default) 1_B: Single ended Write DQS	1,2,3,4,6
Single ended Clock		OP[3]	0_B: Differential Clock (Default), CK_t /CK_c 1_B: Single ended Clock, Only CK_t	1,2,3,4,7

NOTE :
1) The Single-ended mode maximum speed is 800MHz.
2) Device support for single ended mode features (MR51 OP[3:1]) is indicated in MR0 OP[5].
3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
4) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
5) When single ended RDQS mode is enabled (MR51 OP[1] =1B), DRAM drives Read DQSB low or Hi-Z.
6) When single ended WDQS mode is enabled (MR51 OP[2] =1B), Write DQSB is required to be at a valid logic level. A valid Write DQSB signal will meet this requirement.
7) When single ended Clock mode is enabled (MR51 OP[3] =1B), CK_c is required to be at a valid logic level. A valid CK_c signal will meet this requirement.

When DRAM is operating with single-ended mode, both CLKB and write DQSB shall be on "Low" state at all times whereas read DQSB is always on "Hi-Z" state. Refer to the table below.

		Differential Mode	Single-Ended Mode
CLK	CLK	Valid	Valid
	CLKB	Valid	0
Write DQS	DQS	Valid	Valid
	DQSB	Valid	0
Read DQS	DQS	Valid	Valid
	DQSB	Valid	Hi-Z

MR52:63_(RFU) (MA<7:0> = 34_H - $3F_H$) :

6.0 TRUTH TABLES

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4X device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue.
CKE signal has to be held High when the commands listed in the command truth table input.

[Table 12] Command truth table

	SDR Command Pins	SDR CA pins (6)							
SDRAM Command	**CS**	**CA0**	**CA1**	**CA2**	**CA3**	**CA4**	**CA5**	**CK_t edge**	**Notes**
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write-1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write-1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read-1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write-2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write-1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate-1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	V	R10	R11	R2	
Activate-2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

NOTE:

1) All LPDDR4X commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2) “V” means “H” or “L” (a defined logic level). “X” means don’t care in which case CA[5:0] can be floated.
3) Bank addresses BA[2:0] determine which bank is to be operated upon.
4) AB “HIGH” during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don’t care.
5) Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
6) AP “HIGH” during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
7) If Burst Length on-the-fly is enabled, BL “HIGH” during Write-1 or Read-1 command indicates that Burst Length should be set on-the-Fly to BL=32. BL “LOW” during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level “H” or “L”.
8) For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9) Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or mode register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10) Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11) MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12) MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

6.1 CKE Truth Tables

[Table 13] LPDDR4X : CKE Table 1), 2), 3), 4), 8)

Device Current State	CKE$_{n-1}$	CKE$_n$	Command n	Operation	Device Next State	Notes
Active Power Down	L	L	X	Maintain Active Power Down	Active Power Down	
	L	H	Deselect	Exit Active Power Down	Active	5,6
Idle Power Down	L	L	X	Maintain Idle Power Down	Idle Power Down	
	L	H	Deselect	Exit Idle Power Down	Idle	5,6
Self Refresh	L	L	X	Maintain power-down state within Self Refresh	Self Refresh	
	L	H	Deselect	Exit SREF power-down, enable command decode	Self Refresh	5,6,7
	H	L	Deselect	Enter SREF Power-Down, disable command decode	Self Refresh	5,7
	H	H	See Note 7	See Note 7	Self Refresh	7
Bank(s) Active	H	L	Deselect	Enter Active Power Down	Active Power Down	5
All Banks Idle	H	L	Deselect	Enter Idle Power Down	Idle Power Down	5, 8
Command Entry	H	H	Refer to the Command Truth Table			

NOTE :
1) CKE is a strictly asynchronous input, and as such, has no relationship to CK.
2) “X” means “don’t care.”
3) “Current State” is the state of the LPDDR4X-SDRAM prior to a toggle of CKE.
4) “CKEn-1” is the logic state of CKE prior to a CKE toggle event, and “CKEn” is the state of CKE after the toggle event.
5) “Deselect” is the only valid command that can be present on the bus when CKE is toggled.
6) Power-Down exit time (tXP) should elapse before a command other than Deselect is issued. The clock must toggle at least twice during the tXP period, and must be stable before issuing a command.
7) When the device is in Self.Refresh, only MRR, MRW, or MPC commands are allowed. Certain restrictions apply to changing register contents via a MRW command during SREF. See MRW section for more information.
8) In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VSSQ.

6.2 State Truth Table

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

[Table 14] Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	NOTES
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing (All Bank)	7
	MRW	Write value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	8, 13
Row Active	Read	Select column, and start read burst	Reading	10
	Write	Select column, and start write burst	Writing	10
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading	Read	Select column, and start new read burst	Reading	9, 10
	Write	Select column, and start write burst	Writing	9, 10, 11
Writing	Write	Select column, and start new write burst	Writing	9, 10
	Read	Select column, and start read burst	Reading	9, 10, 12

NOTE :

1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.

2) All states and sequences not shown are illegal or reserved.

3) Current State Definitions:
- Idle: The bank or banks have been precharged, and tRP has been met.
- Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accesses are in progress.
- Reading: A Read burst has been initiated, with Auto Precharge disabled.
- Writing: A Write burst has been initiated, with Auto Precharge disabled.

4) The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and LPDDR4 Pad definition and LPDDR4 SDRAM addressing.
- Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
- Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
- Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
- Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5) The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
- Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
- Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
- Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
- Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
- Idle MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
- Active MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Active state.
- Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

6) Bank-specific; requires that the bank is idle and no bursts are in progress.

7) Not bank-specific; requires that all banks are idle and no bursts are in progress.

8) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.

9) A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.

10) The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.

11) A Write command may be applied after the completion of the Read burst; burst terminates are not permitted.

12) A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

13) If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

[Table 15] Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for Bank m	NOTES
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	6
	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7
	Precharge	Deactivate row in bank or banks	Precharging	8
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Reading	9,10
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7
	Write	Select column, and start write burst to Bank m	Writing	7,12
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing/Masked Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	7,14
	Write	Select column, and start write burst to Bank m	Writing	7
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13
	Write	Select column, and start write burst to Bank m	Writing	7,12,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8
Writing/Masked Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	7,13,14
	Write	Select column, and start write burst to Bank m	Writing	7,13
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	8

NOTE :
1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
2) All states and sequences not shown are illegal or reserved.
3) Current State Definitions:
- Idle: The bank has been precharged, and tRP has been met.
- Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
- Reading: A Read burst has been initiated, with Auto Precharge disabled.
- Writing: A Write burst has been initiated, with Auto Precharge disabled

4) Refresh, Self-Refresh, and Mode register Write commands may only be issued when all bank are idle.
5) The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
- Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
- Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
- Idle MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
- Active MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Active state.

6) t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m. Additionally, in the case of multiple banks activated, t_{FAW} must be satisfied.
7) Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
8) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
9) MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when t_{RCD} is met.)
10) MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.)
11) The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
12) A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
13) Read with auto precharge enabled or a Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the Precharge & Auto Precharge clarification table are followed.
14) A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

7.0 ABSOLUTE MAXIMUM DC RATINGS

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 16] Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to V_{SS}	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to V_{SS}	V_{DD2}	-0.4	1.4	V	1
V_{DDQ} supply voltage relative to V_{SSQ}	V_{DDQ}	-0.4	1.4	V	1
Voltage on any ball except V_{DD1} relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.4	V	
Storage Temperature	T_{STG}	-55	125	°C	2

NOTE :
1) See Power Ramp for relationships between power supplies.
2) Storage Temperature is the case surface temperature on the center/top side of the LPDDR4X device. For the measurement conditions, please refer to JESD51-2 standard.

8.0 AC & DC OPERATING CONDITIONS

8.1 Recommended DC Operating Conditions

[Table 17] Recommended DC Operating Conditions

Symbol	DRAM	LPDDR4X			Unit	Notes
		Min	Typ	Max		
VDD1	Core 1 Power	1.70	1.80	1.95	V	1,2
VDD2	Core 2 Power / Input Buffer Power	1.06	1.10	1.17	V	1,2,3
VDDQ	I/O Buffer Power	0.57	0.60	0.65	V	2,3

NOTE :
1) VDD1 uses significantly less current than VDD2.
2) The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3) The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mv at the DRAM ball is not included in the TdIVW.

8.2 Input Leakage Current

[Table 18] Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-8	8	uA	1,2

NOTE :
1) For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ VDD2 (All other pins not under test = 0V).
2) CA ODT is disabled for CK_t, CK_c, CS, and CA.

8.3 Input/Output Leakage Current

[Table 19] Input/Output Leakage Current

Parameter/Condition	Symbol	Min.	Max.	Unit	Notes
Input/Output Leakage current	I_{OZ}	-10	10	uA	1,2

NOTE :
1) For DQ, DQS_t, DQS_c and DMI. Any I/O 0V ≤ V_{OUT} ≤ V_{DDQ}.
2) I/Os status are disabled: High Impedance and ODT Off.

8.4 Operating Temperature Range

[Table 20] Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Standard	T_{OPER}	-25	85	°C

NOTE :
1) Operating Temperature is the case surface temperature on the center top side of the LPDDR4X device. For the measurement conditions, please refer to JESD51-2.
2) Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

9.0 AC AND DC INPUT/OUTPUT MEASUREMENT LEVELS

9.1 1.1V High speed LVCMOS (HS_LLVCMOS)

9.1.1 Standard specifications

All voltages are referenced to ground except where noted.

9.1.2 DC electrical characteristics

9.1.2.1 LPDDR4X Input Level for CKE

This definition applies to CKE_A/B.

[Table 21] LPDDR4X Input Level for CKE

Parameter	Symbol	Min.	Max.	Unit	Note
Input high level (AC)	$V_{IH(AC)}$	0.75 × V_{DD2}	V_{DD2} + 0.2	V	1
Input low level (AC)	$V_{IL(AC)}$	-0.2	0.25 × V_{DD2}	V	1
Input high level (DC)	$V_{IH(DC)}$	0.65 × V_{DD2}	V_{DD2} + 0.2	V	
Input low level (DC)	$V_{IL(DC)}$	-0.2	0.35 × V_{DD2}	V	

NOTE :
1) Refer LPDDR4X AC Over/Undershoot section.

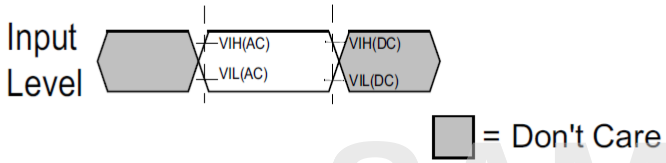


Figure 3. LPDDR4X Input AC timing definition for CKE
1-1). AC level is guaranteed transition point.
1-2). DC level is hysteresis.

9.1.2.2 LPDDR4X Input Level for Reset_n and ODT_CA

This definition applies to Reset_n and ODT_CA.

[Table 22] LPDDR4X Input Level for Reset_n and ODT_CA

Parameter	Symbol	Min.	Max.	Unit	Note
Input high level	VIH	0.80 × V_{DD2}	V_{DD2} + 0.2	V	1
Input low level	VIL	-0.2	0.20× V_{DD2}	V	1

NOTE :
1) Refer LPDDR4X AC Over/Undershoot section.

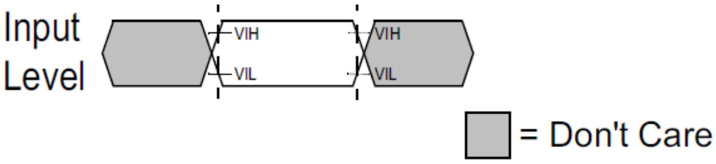


Figure 4. LPDDR4X Input AC timing definition for Reset_n and ODT_CA

9.1.3 AC Over/Undershoot

9.1.3.1 LPDDR4X AC Over/Undershoot

[Table 23] LPDDR4X AC Over/Undershoot

Parameter	Specification
Maximum peak amplitude allowed for overshoot area.	0.35V
Maximum peak amplitude allowed for undershoot area.	0.35V
Maximum overshoot area above V_{DD}/V_{DDQ}.	0.8V-ns
Maximum undershoot area below V_{SS}/V_{SSQ}.	0.8V-ns

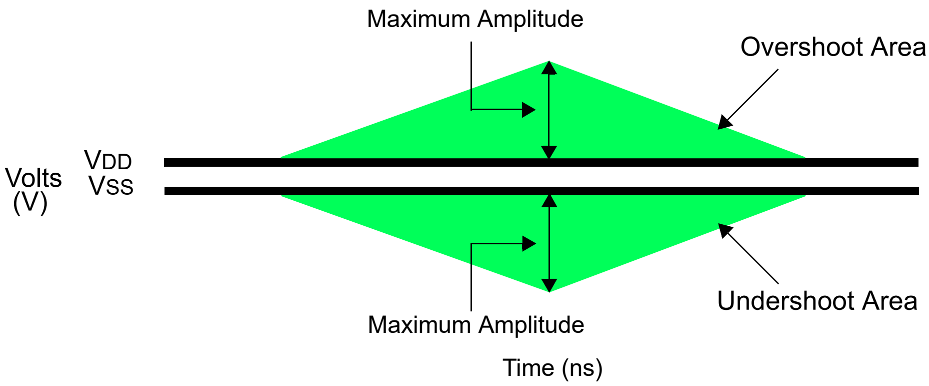


Figure 5. AC Overshoot and Undershoot Definition for Address and Control Pins

9.2 Differential Input Voltage

9.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

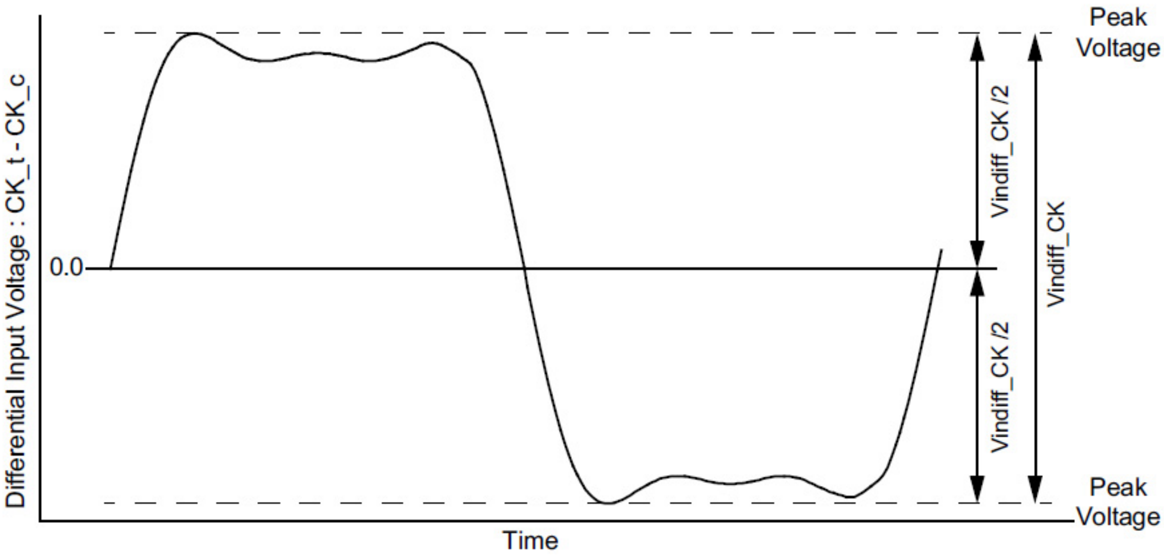


Figure 6. CK Differential Input Voltage

[Table 24] CK differential input voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866 a)		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	Vindiff_CK	420	-	380	-	360	-	mV	1

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

NOTE:

1) The peak voltage of Differential CK signals is calculated in a following equation.
Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

9.2.2 Peak voltage calculation method

The peak voltage of Differential Clock signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

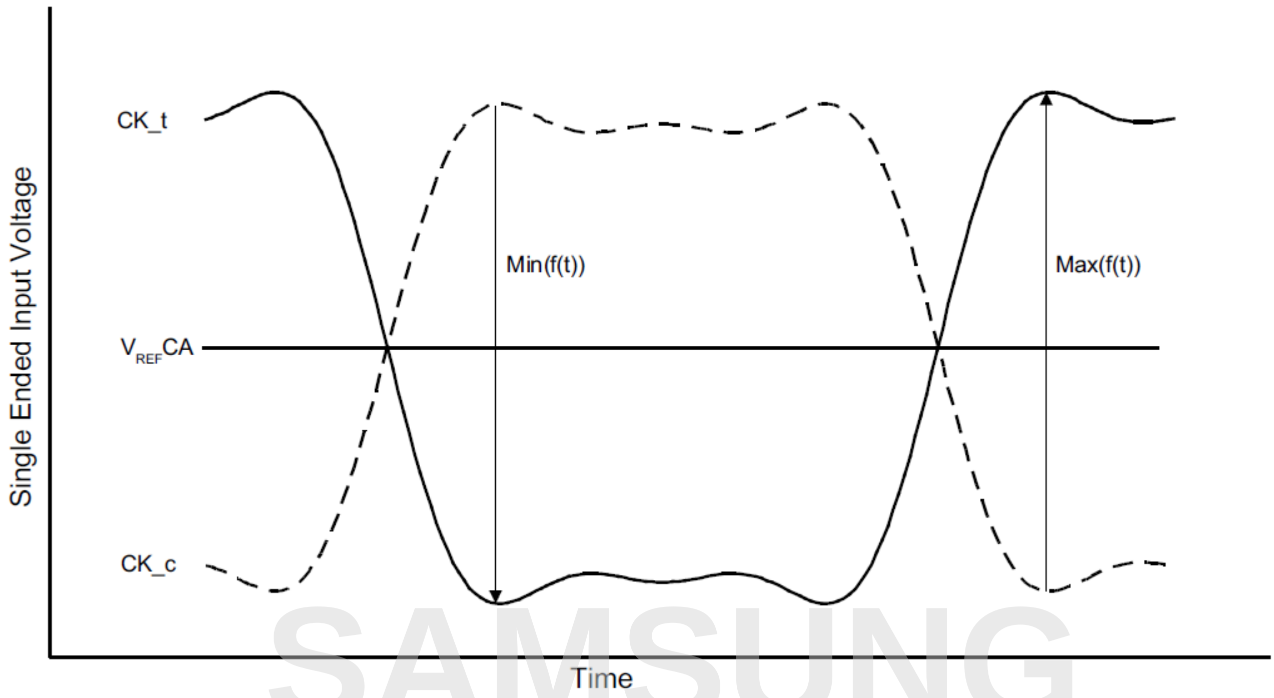


Figure 7. Definition of differential Clock Peak Voltage

NOTE:
1) VREFCA is LPDDR4X SDRAM internal setting value by VREF Training.

9.2.3 Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver.

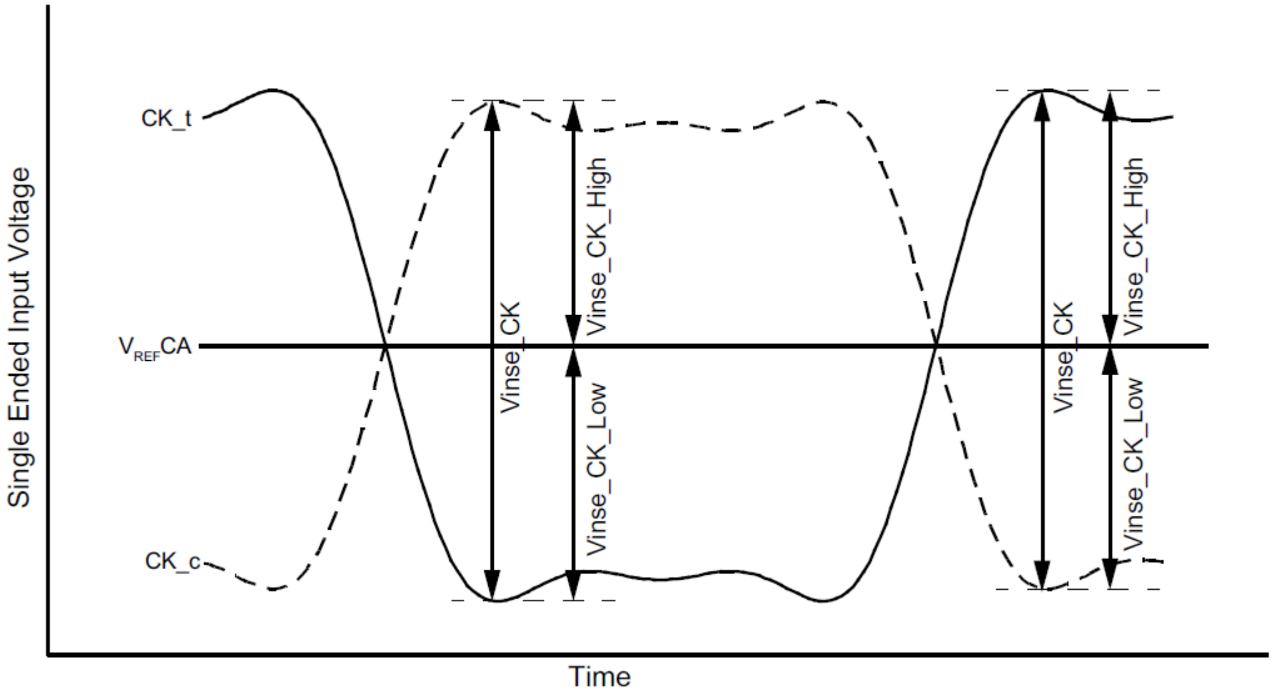


Figure 8. Clock Single-Ended Input Voltage

NOTE:
1) VREFCA is LPDDR4X SDRAM internal setting value by VREF Training.

[Table 25] Clock Single-Ended input voltage

Parameter	Symbol	Data Rate						Unit
		1600/1866 [a]		2133/2400/3200		3733/4266		
		Min	Max	Min	Max	Min	Max	
Clock Single-Ended input voltage	Vinse_CK	210	-	190	-	180	-	mV
Clock Single-Ended input voltage High from VREFDQ	Vinse_CK_High	105	-	95	-	90	-	mV
Clock Single-Ended input voltage Low from VREFDQ	Vinse_CK_Low	105	-	95	-	90	-	mV

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

9.2.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 9. and the following Tables.

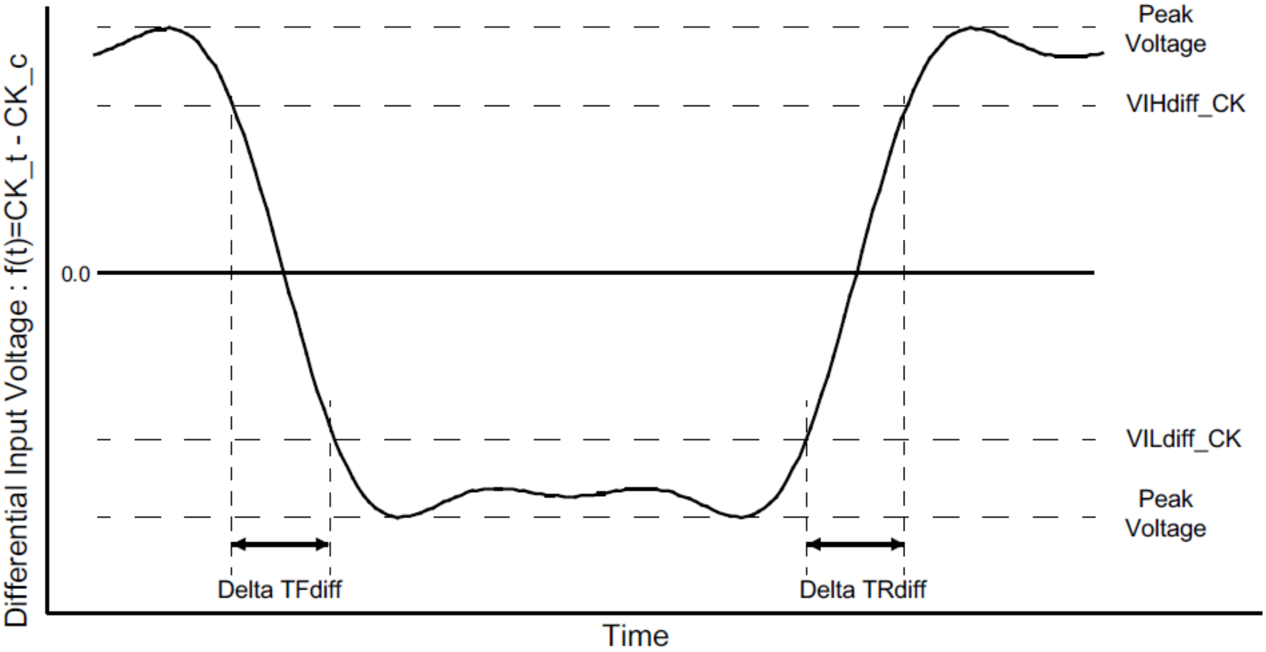


Figure 9. Differential Input Slew Rate Definition for CK_t, CK_c

NOTE :
1) Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
2) Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

[Table 26] Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge (CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTFdiff

[Table 27] Differential Input Level for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866 a)		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input High	VIHdiff_CK	175	-	155	-	145	-	mV	
Differential Input Low	VILdiff_CK	-	-175	-	-155	-	-145	mV	

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

[Table 28] Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	V/ns	

9.2.5 Differential Input Cross Point Voltage for Clock

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 29. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level.

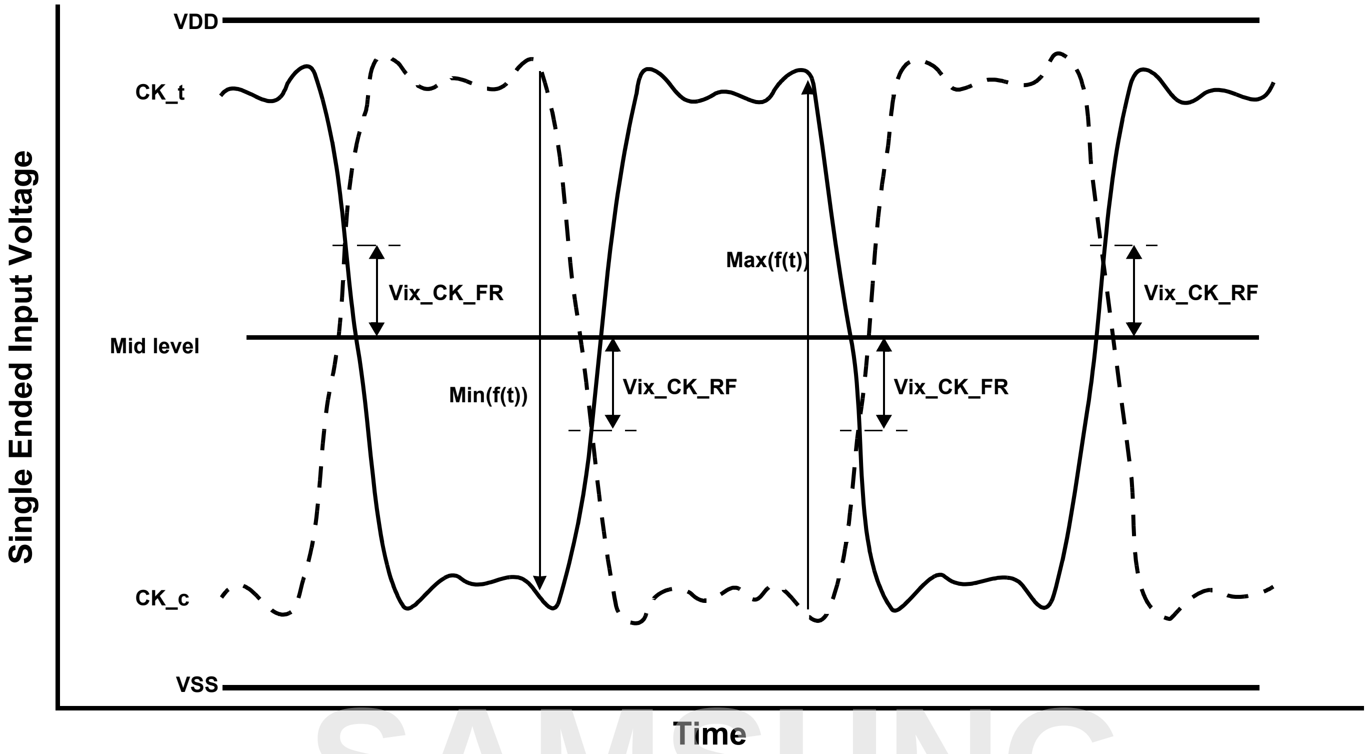


Figure 10. Vix Definition (Clock)

NOTE :
1) The base level of Vix_CK_FR/RF is VREFCA that is LPDDR4X SDRAM internal setting value by VREF Training.

[Table 29] Cross point voltage for differential input signals (Clock)

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866 [a)]		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock Differential input cross point voltage ratio	Vix_CK_ratio	-	25	-	25	-	25	%	1,2

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

NOTE :
1) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
2) Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))
3) Vix_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
Vix_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.
4) In LPDDR4X un-terminated case, CK mid-level is calculated as :
High level=VDDQ, Low level=VSS, Mid-level = VDDQ/2.
In LPDDR4 un-terminated case, Mid-level must be equal or lower than 369mV (33.6% of VDD2).

9.2.6 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

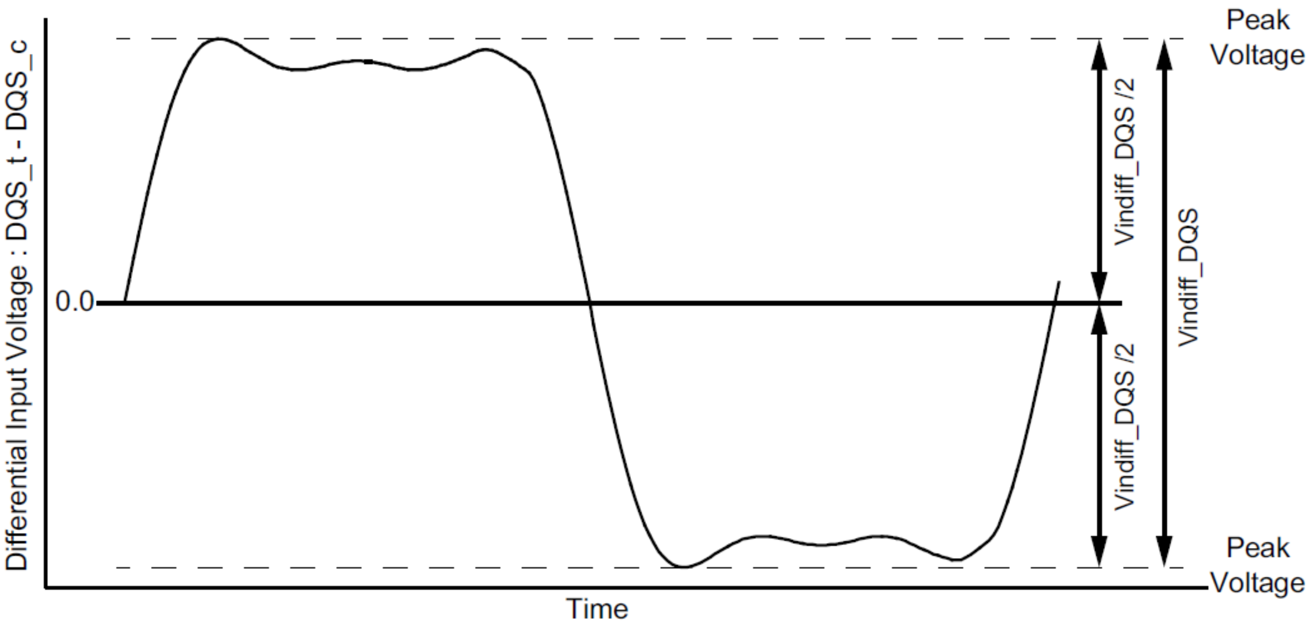


Figure 11. DQS Differential Input Voltage

[Table 30] DQS differential input voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866 [a]		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS differential input	Vindiff_DQS	360	-	360	-	340	-	mV	1

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

NOTE :

1) The peak voltage of Differential DQS signals is calculated in a following equation.
Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
Max Peak Voltage = Max(f(t))
Min Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

9.2.7 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

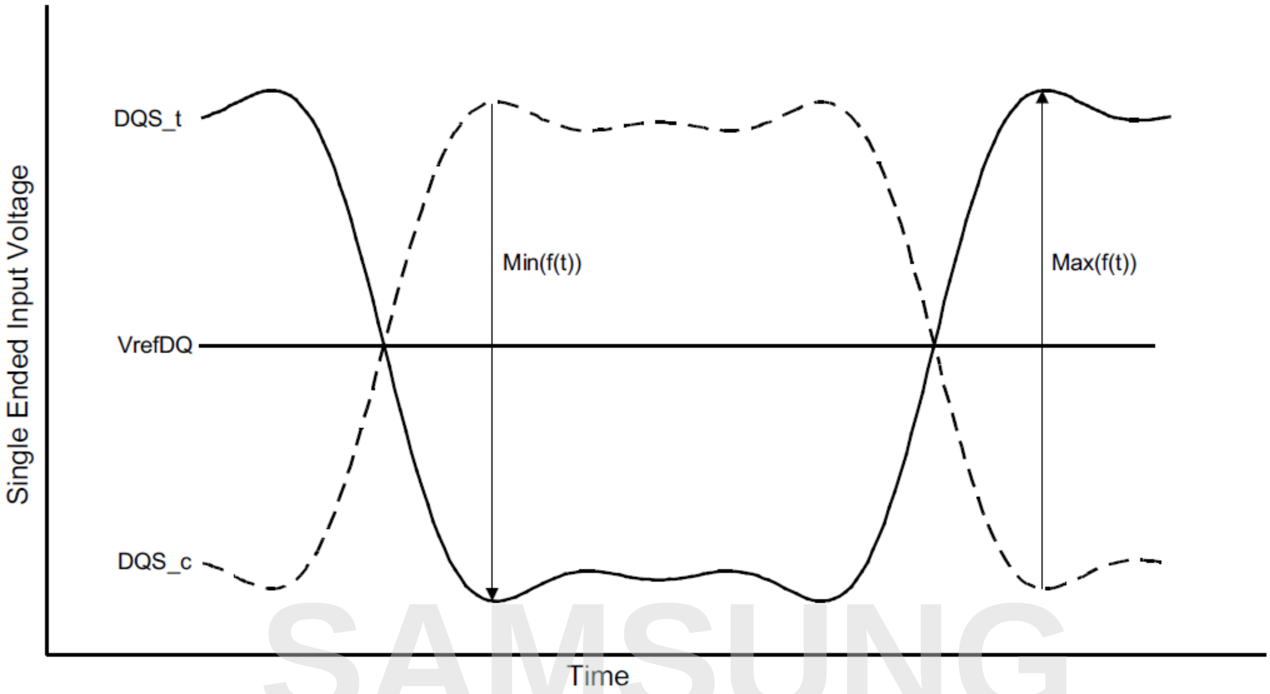


Figure 12. Definition of differential DQS Peak Voltage

NOTE :
1) VrefDQ is LPDDR4X SDRAM internal setting value by Vref Training.

9.2.8 Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both Vinse_DQS, Vinse_DQS_High/Low specification at input receiver.

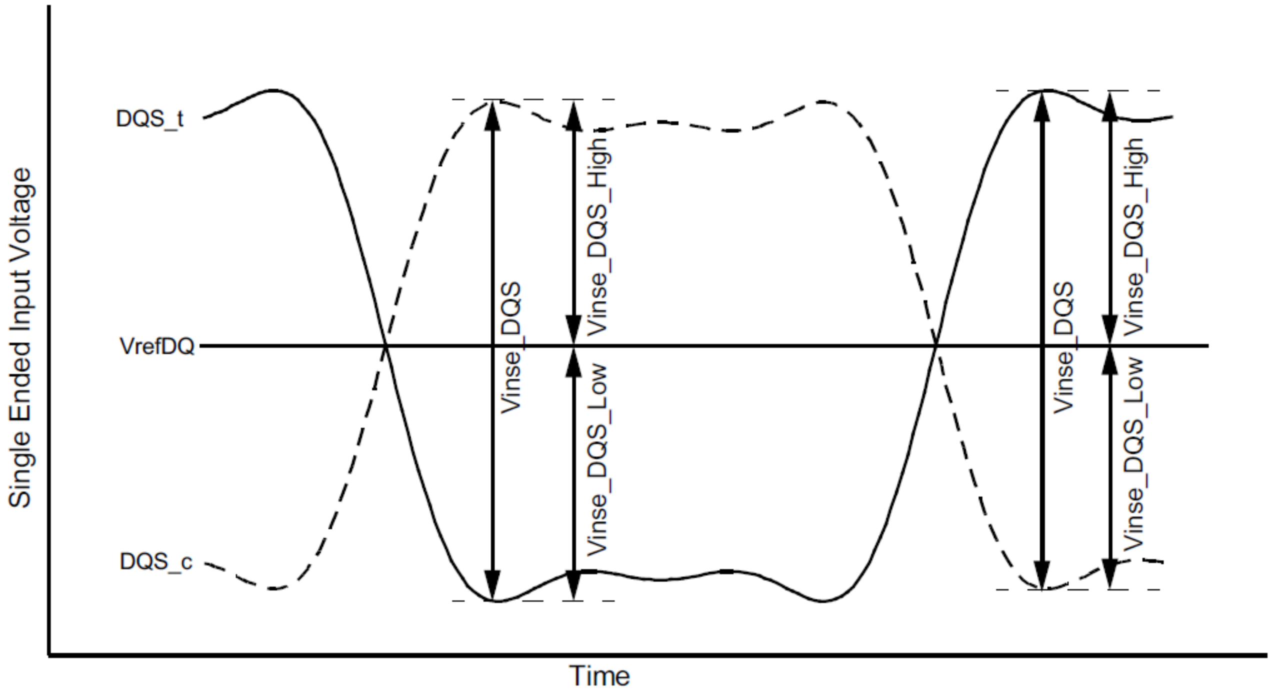


Figure 13. DQS Single-Ended Input Voltage

NOTE :
1) VrefDQ is LPDDR4X SDRAM internal setting value by Vref Training.

[Table 31] DQS Single-Ended input voltage

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866 [a]		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS Single-Ended input voltage	Vinse_DQS	180	-	180	-	170	-	mV	
DQS Single-Ended input voltage High from VrefDQ	Vinse_DQS_High	90	-	90	-	85	-	mV	
DQS Single-Ended input voltage Low from VrefDQ	Vinse_DQS_Low	90	-	90	-	85	-	mV	

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

9.2.9 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 14. and Table 32.

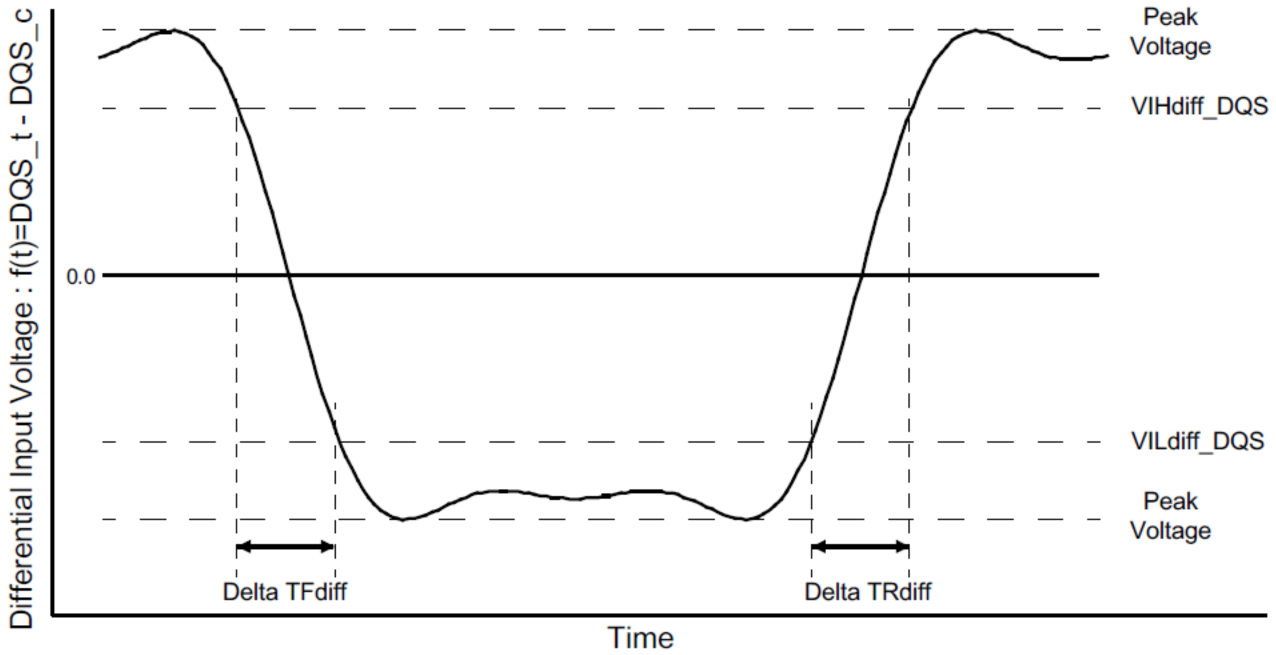


Figure 14. Differential Input Slew Rate Definition for DQS_t, DQS_c

NOTE :
1) Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
2) Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope.

[Table 32] Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge (DQS_t - DQS_c)	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge (DQS_t - DQS_c)	VIHdiff_DQS	VILdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTFdiff

[Table 33] Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866 a)		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input High	VIHdiff_DQS	140	-	140	-	120	-	mV	
Differential Input Low	VILdiff_DQS	-	-140	-	-140	-	-120	mV	

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

[Table 34] Differential Input Slew Rate for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1866		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate	SRIdiff	2	14	2	14	2	14	V/ns	

9.3 Differential Input Cross Point Voltage for DQS

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 35. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is $V_{REF}DQ$.

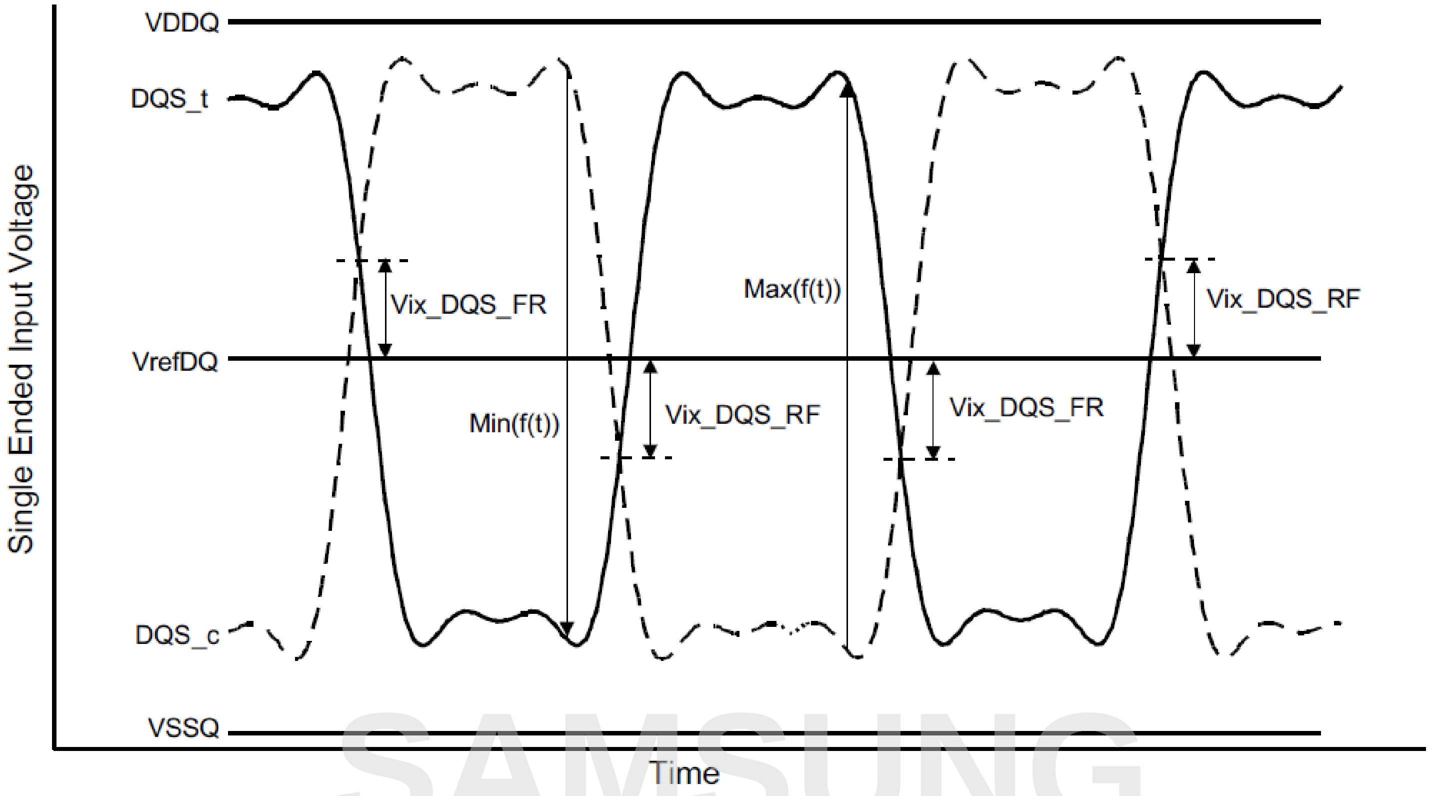


Figure 15. Vix Definition (DQS)

NOTE :
1) The base level of Vix_DQS_FR/RF is VrefDQ that is LPDDR4X SDRAM internal setting value by Vref Training.

[Table 35] Cross point voltage for differential input signals (DQS)

Parameter	Symbol	Data Rate						Units	Notes
		1600/1866 a)		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	20	-	20	-	20	%	1,2

a) The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1866.

NOTE :
1) Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_FR/|Min(f(t))|
2) Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_RF/Max(f(t))

9.4 Single Ended Output Slew Rate

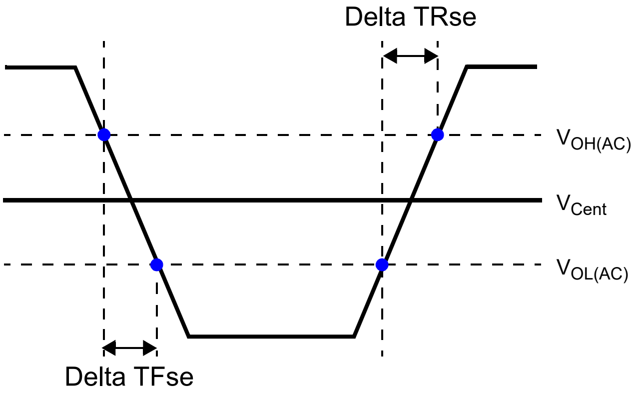


Figure 16. Single Ended Output Slew Rate Definition

[Table 36] Output Slew Rate (single-ended) for 0.6V VDDQ

Parameter	Symbol	Value		Units
		Min[1]	Max[2]	
Single-ended Output Slew Rate (V_{OH} = VDDQ×0.5)	S_{RQse}	3.0	9.0	V/ns
Output slew-rate matching Ratio (Rise to Fall)		0.8	1.2	-

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

NOTE :
1) Measured with output reference load.
2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
3) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = 0.2 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
4) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

9.5 Differential Output Slew Rate

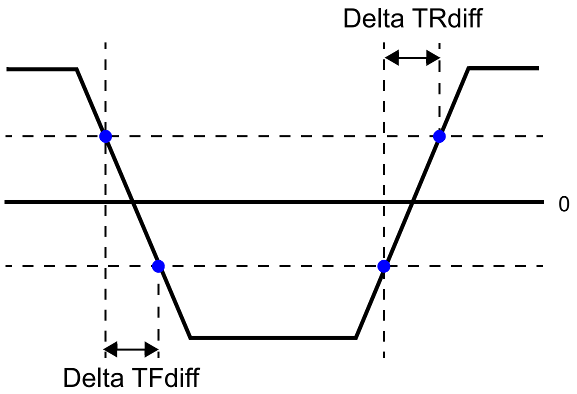


Figure 17. Differential Output Slew Rate Definition

[Table 37] Differential Output Slew Rate for 0.6V VDDQ

Parameter	Symbol	Value		Units
		Min	Max	
Differential Output Slew Rate (V_{OH} = VDDQ×0.5)	SRQdiff	6	18.0	V/ns

Description:

SR: Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

diff: Differential Signals

NOTE :
1) Measured with output reference load.
2) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$=-0.8×$V_{OH(DC)}$ and $V_{OH(AC)}$=0.8×$V_{OH(DC)}$.
3) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

9.6 Overshoot and Undershoot for LVSTL

[Table 38] AC Overshoot/Undershoot Specification

Parameter		Data Rate					Units
		1600	1866	3200	3733	4266	
Maximum peak amplitude allowed for overshoot area. (See Figure 18.)	Max	0.3	0.3	0.3	0.3	0.3	V
Maximum peak amplitude allowed for undershoot area. (See Figure 18.)	Max	0.3	0.3	0.3	0.3	0.3	V
Maximum overshoot area above V_{DD}. (See Figure 18.)	Max	0.1	0.1	0.1	0.1	0.1	V-ns
Maximum undershoot area below V_{SS}. (See Figure 18.)	Max	0.1	0.1	0.1	0.1	0.1	V-ns

NOTE :

1) V_{DD2} stands for V_{DD} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{DD} stands for V_{DDQ} for DQ, DMI, DQS_t and DQS_c.
2) V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{SS} stands for V_{SSQ} for DQ, DMI, DQS_t and DQS_c.
3) Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
4) Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

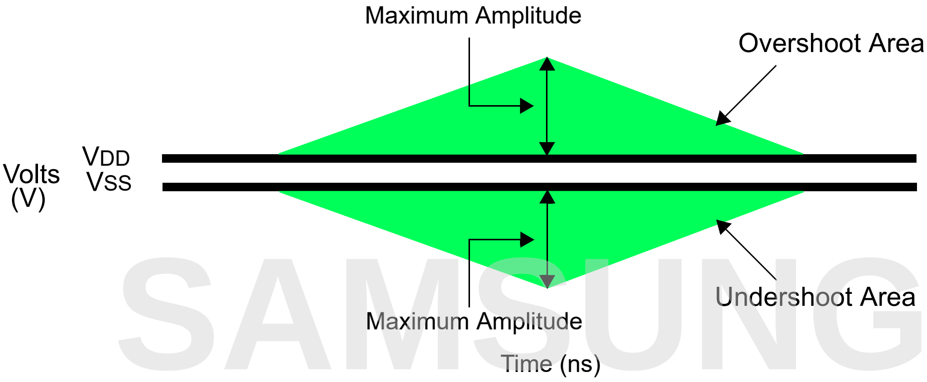


Figure 18. Overshoot and Undershoot Definition

9.7 LPDDR4X Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

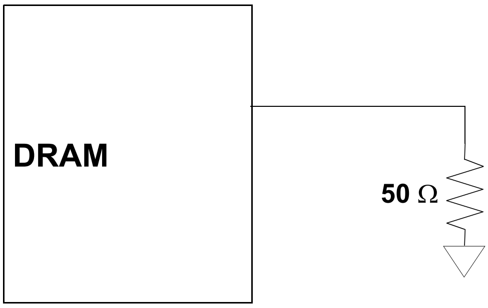


Figure 19. Driver Output Reference Load for Timing and Slew Rate

NOTE :
1) All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

9.8 LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in Figure 20 .

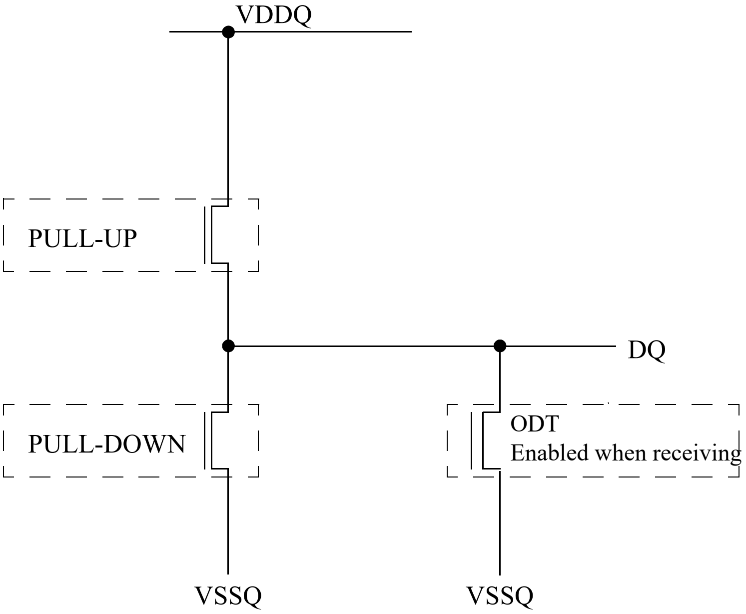


Figure 20. LVSTL I/O Cell

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to calibrated as below procedure.

1) First calibrate the pull-down device against a 240 Ohm resister to VDDQ via the ZQ pin
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is less than VDDQ/2.
- NMOS pull-down device is calibrated to 240 Ohms

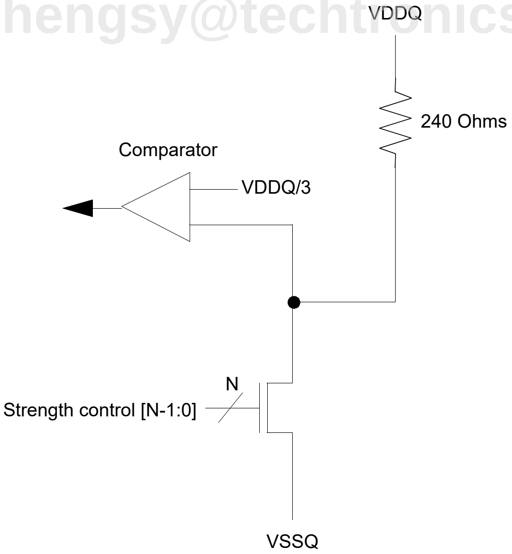


Figure 21. pull-down calibration

2) Then calibrate the pull-up device against the calibrated pull-down device.
- Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)
- Set Strength Control to minimum setting
- Increase drive strength until comparator detects data bit is greater than VOH target
- NMOS pull-up device is now calibrated to VOH target

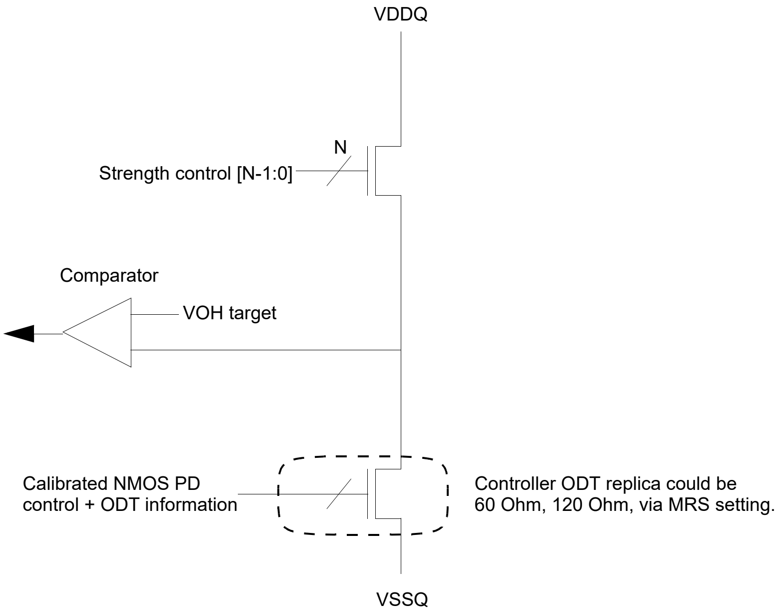


Figure 22. pull-up calibration

10.0 INPUT/OUTPUT CAPACITANCE

[Table 39] Input/Output Capacitance

Parameter	Symbol	Min/Max	Value	Unit	Notes
Input capacitance, CK_t and CK_c	CCK	Min	1.1	pF	1,2
		Max	3.1		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	pF	1,2,3
		Max	0.2		
Input capacitance, all other input-only pins except CS and CKE	CI1	Min	1.1	pF	1,2,4
		Max	3.1		
Cin, CS0 / CS1 and CKE0 / CKE1	CI2	Min	0.5	pF	1,2,4
		Max	2.5		
Input capacitance delta, all other input-only pins except CS and CKE	CDI1	Min	-0.3	pF	1,2,5
		Max	0.3		
Cdelta, CS0 / CS1 and CKE0 / CKE1	CDI2	Min	-0.6	pF	1,2,5,9
		Max	0.6		
Input/output capacitance, DQ, DMI, DQS_t and DQS_c	CIO	Min	1.6	pF	1,2,6
		Max	3.6		
Input/output capacitance delta, DQS_t and DQS_c	CDDQS	Min	0.0	pF	1,2,7
		Max	0.3		
Input/output capacitance delta, DQ and DMI	CDIO	Min	-0.6	pF	1,2,8
		Max	0.6		
Input/output capacitance ZQ pin	CZQ	Min	4.0	pF	1,2
		Max	8.0		

NOTE :
1) This parameter applies to both die and package.
2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating.
3) Absolute value of CCK_t - CCK_c.
4) CI applies to CS_n, CKE, CA0-CA5.
5) CDI = CI - 0.5 × (CCK_t + CCK_c)
6) DMI loading matches DQ and DQS.
7) Absolute value of CDQS_t and CDQS_c.
8) CDIO = CIO - 0.5 × (CDQS_t + CDQS_c) in byte-lane.
9) CDI2 = CI2 - 0.25 × (CCK_t + CCK_c).

11.0 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

11.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

- LOW: $V_{IN} \le V_{IL}$(DC) MAX
- HIGH: $V_{IN} \ge V_{IH}$(DC) MIN
- STABLE: Inputs are stable at a HIGH or LOW level
- SWITCHING: See Table 40 and Table 41.

[Table 40] Definition of Switching for CA Input Signals

Switching for CA								
CK_t edge	R1	R2	R3	R4	R5	R6	R7	R8
CKE	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH
CS	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

NOTE :
1) CS must always be driven LOW.
2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3) The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

[Table 41] CA pattern for IDD4R for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		H	H	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :
1) BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B, Burst Order CA[3:2] = 00_B or 11_B (Same as LPDDR3 IDD4R Spec)
2) Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.

[Table 42] CA pattern for IDD4W for BL=16

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+9	HIGH	LOW		L	H	L	L	H	L
N+10	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+11	HIGH	LOW		L	L	H	H	H	H
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :
1) BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B (Same as LPDDR3 IDD4W Spec.)
2) Difference from LPDDR3 Spec :
  1-No burst ordering
  2-CA pins are kept low with DES CMD to reduce ODT current.

[Table 43] Data Pattern for IDD4W (DBI off) for BL=16

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE:
1) Simplified pattern compared with last showing.
Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 44] Data Pattern for IDD4R (DBI off) for BL=16

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	1	1	0	8
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	1	1	1	1	1	1	0	0	0	6
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	1	1	0	8
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	1	1	1	1	1	1	0	0	0	6
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	16	16		

NOTE:
1) Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 45] Data Pattern for IDD4W (DBI on) for BL=16

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
No. of 1's	8	8	8	8	8	8	16	16	8	

🟩 DBI enabled burst

[Table 46] Data Pattern for IDD4R (DBI on) for BL=16

	DBI ON Case									No. of 1’s
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	0	0	1	1
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	0	0	0	0
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	1	1	1	3
BL21	1	1	1	1	0	0	0	0	0	4
BL22	0	0	0	0	0	0	1	1	0	2
BL23	0	0	0	0	1	1	1	1	0	4
BL24	0	0	0	0	0	0	0	0	0	0
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	0	0	1	1
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	1	1	0	2
BL29	0	0	0	0	1	1	1	1	0	4
BL30	0	0	0	0	0	0	1	1	1	3
BL31	1	1	1	1	0	0	0	0	0	4
No. of 1’s	8	8	8	8	8	8	16	16	8	

[Table 47] CA pattern for IDD4R for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Read-1	L	H	L	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		H	H	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :

1) BA[2:0] = 010B, CA[9:5] = 00000B or 11111B, Burst Order CA[4:2] = 000B or 111B.

[Table 48] CA pattern for IDD4W for BL=32

Clock Cycle Number	CKE	CS	Command	CA0	CA1	CA2	CA3	CA4	CA5
N	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+1	HIGH	LOW		L	H	L	L	L	L
N+2	HIGH	HIGH	CAS-2	L	H	L	L	H	L
N+3	HIGH	LOW		L	L	L	L	L	L
N+4	HIGH	LOW	DES	L	L	L	L	L	L
N+5	HIGH	LOW	DES	L	L	L	L	L	L
N+6	HIGH	LOW	DES	L	L	L	L	L	L
N+7	HIGH	LOW	DES	L	L	L	L	L	L
N+8	HIGH	LOW	DES	L	L	L	L	L	L
N+9	HIGH	LOW	DES	L	L	L	L	L	L
N+10	HIGH	LOW	DES	L	L	L	L	L	L
N+11	HIGH	LOW	DES	L	L	L	L	L	L
N+12	HIGH	LOW	DES	L	L	L	L	L	L
N+13	HIGH	LOW	DES	L	L	L	L	L	L
N+14	HIGH	LOW	DES	L	L	L	L	L	L
N+15	HIGH	LOW	DES	L	L	L	L	L	L
N+16	HIGH	HIGH	Write-1	L	L	H	L	L	L
N+17	HIGH	LOW		L	H	L	L	H	L
N+18	HIGH	HIGH	CAS-2	L	H	L	L	H	H
N+19	HIGH	LOW		L	L	L	H	H	H
N+20	HIGH	LOW	DES	L	L	L	L	L	L
N+21	HIGH	LOW	DES	L	L	L	L	L	L
N+22	HIGH	LOW	DES	L	L	L	L	L	L
N+23	HIGH	LOW	DES	L	L	L	L	L	L
N+24	HIGH	LOW	DES	L	L	L	L	L	L
N+25	HIGH	LOW	DES	L	L	L	L	L	L
N+26	HIGH	LOW	DES	L	L	L	L	L	L
N+27	HIGH	LOW	DES	L	L	L	L	L	L
N+28	HIGH	LOW	DES	L	L	L	L	L	L
N+29	HIGH	LOW	DES	L	L	L	L	L	L
N+30	HIGH	LOW	DES	L	L	L	L	L	L
N+31	HIGH	LOW	DES	L	L	L	L	L	L

NOTE :

1) BA[2:0] = 010B, CA[9:5] = 00000B or 11111B.

[Table 49] Data Pattern for IDD4W (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	1	1	1	1	1	1	1	1	0	8
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4

[Table 49] Data Pattern for IDD4W (DBI off) for BL=32

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL36	0	0	0	0	0	0	1	1	0	2
BL37	0	0	0	0	1	1	1	1	0	4
BL38	1	1	1	1	1	1	0	0	0	6
BL39	1	1	1	1	0	0	0	0	0	4
BL40	1	1	1	1	1	1	1	1	0	8
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	1	1	1	1	1	1	0	0	0	6
BL47	1	1	1	1	0	0	0	0	0	4
BL48	1	1	1	1	1	1	0	0	0	6
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	1	1	1	1	1	1	1	1	0	8
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	0	0	0	6
BL59	1	1	1	1	0	0	0	0	0	4
BL60	1	1	1	1	1	1	1	1	0	8
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1's	32	32	32	32	32	32	32	32		

NOTE :

1) Simplified pattern compared with last showing.
Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 50] Data Pattern for IDD4R (DBI off) for BL=32

	DBI OFF Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	1	1	1	1	1	1	1	1	0	8
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	1	1	1	1	1	1	0	0	0	6
BL7	1	1	1	1	0	0	0	0	0	4
BL8	1	1	1	1	1	1	1	1	0	8
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	1	1	1	1	1	1	0	0	0	6
BL15	1	1	1	1	0	0	0	0	0	4
BL16	1	1	1	1	1	1	0	0	0	6
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	1	1	1	1	1	1	1	1	0	8
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	1	1	1	1	1	1	0	0	0	6
BL27	1	1	1	1	0	0	0	0	0	4
BL28	1	1	1	1	1	1	1	1	0	8
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	1	1	1	1	1	1	0	0	0	6
BL35	1	1	1	1	0	0	0	0	0	4

[Table 50] Data Pattern for IDD4R (DBI off) for BL=32

DBI OFF Case										No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL36	1	1	1	1	1	1	1	1	0	8
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4
BL42	1	1	1	1	1	1	0	0	0	6
BL43	1	1	1	1	0	0	0	0	0	4
BL44	1	1	1	1	1	1	1	1	0	8
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	1	1	1	1	1	1	1	1	0	8
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	1	1	1	1	1	1	0	0	0	6
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	1	1	1	1	1	1	1	1	0	8
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	1	1	1	1	1	1	0	0	0	6
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1's	32	32	32	32	32	32	32	32		

NOTE :

1) Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 51] Data Pattern for IDD4W (DBI on) for BL=32

	DBI ON Case									No. of 1’s
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	0	0	1	1
BL33	1	1	1	1	0	0	0	0	0	4
BL34	0	0	0	0	0	0	0	0	0	0
BL35	0	0	0	0	1	1	1	1	0	4
BL36	0	0	0	0	0	0	1	1	0	2

[Table 51] Data Pattern for IDD4W (DBI on) for BL=32

DBI ON Case										No. of 1’s
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL37	0	0	0	0	1	1	1	1	0	4
BL38	0	0	0	0	0	0	1	1	1	3
BL39	1	1	1	1	0	0	0	0	0	4
BL40	0	0	0	0	0	0	0	0	1	1
BL41	1	1	1	1	0	0	0	0	0	4
BL42	0	0	0	0	0	0	0	0	0	0
BL43	0	0	0	0	1	1	1	1	0	4
BL44	0	0	0	0	0	0	1	1	0	2
BL45	0	0	0	0	1	1	1	1	0	4
BL46	0	0	0	0	0	0	1	1	1	3
BL47	1	1	1	1	0	0	0	0	0	4
BL48	0	0	0	0	0	0	1	1	1	3
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	1	1	0	2
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	0	0	0	0
BL53	0	0	0	0	1	1	1	1	0	4
BL54	0	0	0	0	0	0	0	0	1	1
BL55	1	1	1	1	0	0	0	0	0	4
BL56	0	0	0	0	0	0	1	1	0	2
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	1	1	1	3
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	0	0	1	1
BL61	1	1	1	1	0	0	0	0	0	4
BL62	0	0	0	0	0	0	0	0	0	0
BL63	0	0	0	0	1	1	1	1	0	4
No. of 1’s	16	16	16	16	16	16	32	32	16	

🟩 DBI enabled burst

[Table 52] Data Pattern for IDD4R (DBI on) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL0	0	0	0	0	0	0	0	0	1	1
BL1	1	1	1	1	0	0	0	0	0	4
BL2	0	0	0	0	0	0	0	0	0	0
BL3	0	0	0	0	1	1	1	1	0	4
BL4	0	0	0	0	0	0	1	1	0	2
BL5	0	0	0	0	1	1	1	1	0	4
BL6	0	0	0	0	0	0	1	1	1	3
BL7	1	1	1	1	0	0	0	0	0	4
BL8	0	0	0	0	0	0	0	0	1	1
BL9	1	1	1	1	0	0	0	0	0	4
BL10	0	0	0	0	0	0	0	0	0	0
BL11	0	0	0	0	1	1	1	1	0	4
BL12	0	0	0	0	0	0	1	1	0	2
BL13	0	0	0	0	1	1	1	1	0	4
BL14	0	0	0	0	0	0	1	1	1	3
BL15	1	1	1	1	0	0	0	0	0	4
BL16	0	0	0	0	0	0	1	1	1	3
BL17	1	1	1	1	0	0	0	0	0	4
BL18	0	0	0	0	0	0	1	1	0	2
BL19	0	0	0	0	1	1	1	1	0	4
BL20	0	0	0	0	0	0	0	0	0	0
BL21	0	0	0	0	1	1	1	1	0	4
BL22	0	0	0	0	0	0	0	0	1	1
BL23	1	1	1	1	0	0	0	0	0	4
BL24	0	0	0	0	0	0	1	1	0	2
BL25	0	0	0	0	1	1	1	1	0	4
BL26	0	0	0	0	0	0	1	1	1	3
BL27	1	1	1	1	0	0	0	0	0	4
BL28	0	0	0	0	0	0	0	0	1	1
BL29	1	1	1	1	0	0	0	0	0	4
BL30	0	0	0	0	0	0	0	0	0	0
BL31	0	0	0	0	1	1	1	1	0	4
BL32	0	0	0	0	0	0	1	1	0	2
BL33	0	0	0	0	1	1	1	1	0	4
BL34	0	0	0	0	0	0	1	1	1	3
BL35	1	1	1	1	0	0	0	0	0	4
BL36	0	0	0	0	0	0	0	0	1	1
BL37	1	1	1	1	0	0	0	0	0	4
BL38	0	0	0	0	0	0	0	0	0	0
BL39	0	0	0	0	1	1	1	1	0	4
BL40	0	0	0	0	0	0	1	1	0	2
BL41	0	0	0	0	1	1	1	1	0	4

[Table 52] Data Pattern for IDD4R (DBI on) for BL=32

	DBI ON Case									No. of 1's
	DQ[7]	DQ[6]	DQ[5]	DQ[4]	DQ[3]	DQ[2]	DQ[1]	DQ[0]	DBI	
BL42	0	0	0	0	0	0	1	1	1	3
BL43	1	1	1	1	0	0	0	0	0	4
BL44	0	0	0	0	0	0	0	0	1	1
BL45	1	1	1	1	0	0	0	0	0	4
BL46	0	0	0	0	0	0	0	0	0	0
BL47	0	0	0	0	1	1	1	1	0	4
BL48	0	0	0	0	0	0	0	0	1	1
BL49	1	1	1	1	0	0	0	0	0	4
BL50	0	0	0	0	0	0	0	0	0	0
BL51	0	0	0	0	1	1	1	1	0	4
BL52	0	0	0	0	0	0	1	1	1	3
BL53	1	1	1	1	0	0	0	0	0	4
BL54	0	0	0	0	0	0	1	1	0	2
BL55	0	0	0	0	1	1	1	1	0	4
BL56	0	0	0	0	0	0	0	0	0	0
BL57	0	0	0	0	1	1	1	1	0	4
BL58	0	0	0	0	0	0	0	0	1	1
BL59	1	1	1	1	0	0	0	0	0	4
BL60	0	0	0	0	0	0	1	1	0	2
BL61	0	0	0	0	1	1	1	1	0	4
BL62	0	0	0	0	0	0	1	1	1	3
BL63	1	1	1	1	0	0	0	0	0	4
No. of 1's	16	16	16	16	16	16	32	32	16	

11.2 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire elevated temperature range.

[Table 53] LPDDR4X IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Operating one bank active-precharge current: $t_{CK} = t_{CKmin}$; $t_{RC} = t_{RCmin}$; CKE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD0_1$	VDD1	1,10,11
	$IDD0_2$	VDD2	1,10,11
	$IDD0_Q$	VDDQ	1,3,10,11
Idle power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2P_1$	VDD1	1,10,11
	$IDD2P_2$	VDD2	1,10,11
	$IDD2P_Q$	VDDQ	1,3,10,11
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2PS_1$	VDD1	1,10,11
	$IDD2PS_2$	VDD2	1,10,11
	$IDD2PS_Q$	VDDQ	1,3,10,11
Idle non power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD2N_1$	VDD1	1,10,11
	$IDD2N_2$	VDD2	1,10,11
	$IDD2N_Q$	VDDQ	1,3,10,11
Idle non power-down standby current with clock stopped: CK_t = LOW; CK_c = HIGH; CKE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD2NS_1$	VDD1	1,10,11
	$IDD2NS_2$	VDD2	1,10,11
	$IDD2NS_Q$	VDDQ	1,3,10,11
Active power-down standby current: $t_{CK} = t_{CKmin}$; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3P_1$	VDD1	1,10,11
	$IDD3P_2$	VDD2	1,10,11
	$IDD3P_Q$	VDDQ	1,3,10,11
Active power-down standby current with clock stop: CK_t = LOW, CK_c = HIGH; CKE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3PS_1$	VDD1	1,10,11
	$IDD3PS_2$	VDD2	1,10,11
	$IDD3PS_Q$	VDDQ	1,4,10,11

[Table 53] LPDDR4X IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled	$IDD3N_1$	VDD1	1,10,11
	$IDD3N_2$	VDD2	1,10,11
	$IDD3N_Q$	VDDQ	1,4,10,11
Active non-power-down standby current with clock stopped: CK_t=LOW, CK_c=HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$IDD3NS_1$	VDD1	1,10,11
	$IDD3NS_2$	VDD2	1,10,11
	$IDD3NS_Q$	VDDQ	1,4,10,11
Operating burst READ current: $t_{CK} = t_{CKmin}$; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4R_1$	VDD1	1,10,11
	$IDD4R_2$	VDD2	1,10,11
	$IDD4R_Q$	VDDQ	1,5,10,11
Operating burst WRITE current: $t_{CK} = t_{CKmin}$; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled	$IDD4W_1$	VDD1	1,10,11
	$IDD4W_2$	VDD2	1,10,11
	$IDD4W_Q$	VDDQ	1,4,10,11
All-bank REFRESH Burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5_1$	VDD1	1,10,11
	$IDD5_2$	VDD2	1,10,11
	$IDD5_Q$	VDDQ	1,4,10,11
All-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5AB_1$	VDD1	1,10,11
	$IDD5AB_2$	VDD2	1,10,11
	$IDD5AB_Q$	VDDQ	1,4,10,11
Per-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled	$IDD5PB_1$	VDD1	1,10,11
	$IDD5PB_2$	VDD2	1,10,11
	$IDD5PB_Q$	VDDQ	1,4,10,11
Power Down Self refresh current (-25°C to +85°C): CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled	$IDD6_1$	VDD1	6,7,9,10,11
	$IDD6_2$	VDD2	6,7,9,10,11
	$IDD6_Q$	VDDQ	4,6,7,9,10,11

NOTE :
1) Published IDD values are the maximum of the distribution of the arithmetic mean.
2) ODT disabled: MR11[2:0] = 000_B.
3) IDD current specifications are tested after the device is properly initialized.
4) Measured currents are the summation of VDDQ and VDD2.
5) Guaranteed by design with output load = 5pF and RON = 40 ohm.
6) The 1x Self-Refresh Rate is the rate at which the LPDDR4X device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
7) This is the general definition that applies to full array Self Refresh.
8) For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
9) IDD6 25°C is guaranteed, IDD6 85°C is typical of the distribution of the arithmetic mean.
10) These specification values are the summation of all the channel current and both channels are under the same condition at the same time.
11) Dual Channel devices are specified in dual channel operation (both channels operating together).

11.3 IDD Spec Table

[Table 54] IDD Specification for 16Gb LPDDR4X

Symbol		Power Supply	16Gb (x16/Ch, 2-Chip)	Units
			4266Mbps	
IDD0	IDD0$_1$	VDD1	10	mA
	IDD0$_2$	VDD2	65	mA
	IDD0$_Q$	VDDQ	0.5	mA
IDD2P	IDD2P$_1$	VDD1	2	mA
	IDD2P$_2$	VDD2	6.25	mA
	IDD2P$_Q$	VDDQ	0.5	mA
IDD2PS	IDD2PS$_1$	VDD1	2	mA
	IDD2PS$_2$	VDD2	6.25	mA
	IDD2PS$_Q$	VDDQ	0.5	mA
IDD2N	IDD2N$_1$	VDD1	3	mA
	IDD2N$_2$	VDD2	26.5	mA
	IDD2N$_Q$	VDDQ	0.5	mA
IDD2NS	IDD2NS$_1$	VDD1	3	mA
	IDD2NS$_2$	VDD2	20.5	mA
	IDD2NS$_Q$	VDDQ	0.5	mA
IDD3P	IDD3P$_1$	VDD1	2.8	mA
	IDD3P$_2$	VDD2	13.5	mA
	IDD3P$_Q$	VDDQ	0.5	mA
IDD3PS	IDD3PS$_1$	VDD1	2.8	mA
	IDD3PS$_2$	VDD2	13.5	mA
	IDD3PS$_Q$	VDDQ	0.5	mA
IDD3N	IDD3N$_1$	VDD1	3	mA
	IDD3N$_2$	VDD2	34	mA
	IDD3N$_Q$	VDDQ	0.5	mA
IDD3NS	IDD3NS$_1$	VDD1	3	mA
	IDD3NS$_2$	VDD2	30	mA
	IDD3NS$_Q$	VDDQ	0.5	mA
IDD4R	IDD4R$_1$	VDD1	46	mA
	IDD4R$_2$	VDD2	465	mA
	IDD4R$_Q$	VDDQ	185	mA
IDD4W	IDD4W$_1$	VDD1	41	mA
	IDD4W$_2$	VDD2	460	mA
	IDD4W$_Q$	VDDQ	0.5	mA
IDD5	IDD5$_1$	VDD1	75	mA
	IDD5$_2$	VDD2	300	mA
	IDD5$_Q$	VDDQ	0.5	mA
IDD5AB	IDD5AB$_1$	VDD1	7	mA
	IDD5AB$_2$	VDD2	40	mA
	IDD5AB$_Q$	VDDQ	0.5	mA

[Table 54] IDD Specification for 16Gb LPDDR4X

Symbol			Power Supply	16Gb (x16/Ch, 2-Chip)	Units
				4266Mbps	
IDD5PB	$IDD5PB_1$		VDD1	7	mA
	$IDD5PB_2$		VDD2	41	mA
	$IDD5PB_Q$		VDDQ	0.5	mA
IDD6	$IDD6_1$	25°C	VDD1	1	mA
		85°C		5	
	$IDD6_2$	25°C	VDD2	2.7	mA
		85°C		22	
	$IDD6_Q$	25°C	VDDQ	0.4	mA
		85°C		0.5	

12.0 AC AND DC OUTPUT MEASUREMENT LEVELS

12.1 Single Ended AC and DC Output Levels

Table 55 shows the output levels used for measurements of single ended signals.

[Table 55] Single-ended AC and DC Output Levels

Symbol	Parameter	Value			Unit	Notes
		Under LPDDR4X-TBD Un-term	TBD to 3200 VSSQ term	3200 to 4266 VSSQ term		
V_{OH} (DC)	AC, DC output high measurement level	VDDQ	VDDQ/2	VDDQ/2	V	1
V_{OL} (DC)	AC, DC output low measurement level	VSSQ	VSSQ	VSSQ	V	

NOTE :
1) 60ohm ODT value is assumed.

12.2 Pull Up/Pull Down Driver Characteristics and Calibration

[Table 56] Pull-down Driver Characteristics, with ZQ Calibration

$R_{ONPD,NOM}$	Resistor	Min	Nom	Max	Unit
40 Ohm	R_{ON40PD}	0.9	1.0	1.1	$R_{ZQ/6}$
48 Ohm	R_{ON48PD}	0.9	1.0	1.1	$R_{ZQ/5}$
60 Ohm	R_{ON60PD}	0.9	1.0	1.1	$R_{ZQ/4}$
80 Ohm	R_{ON80PD}	0.9	1.0	1.1	$R_{ZQ/3}$
120 Ohm	$R_{ON120PD}$	0.9	1.0	1.1	$R_{ZQ/2}$
240 Ohm	$R_{ON240PD}$	0.9	1.0	1.1	$R_{ZQ/1}$

NOTE :
1) All value are after ZQ Calibration. Without ZQ Calibration RONPD values are ± 30%.

[Table 57] Terminated Pull-up Characteristics, with ZQ Calibration

VOH_{PU}, nom	VOH,nom (mV)	Min	Nor	Max	Unit
VDDQ×0.5	300	0.90	1.0	1.10	VOH,nom
VDDQ×0.6	360	0.90	1.0	1.10	VOH,nom

NOTE :
1) All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%
2) VOH,nom (mV) values are based on a nominal VDDQ = 0.6V.

[Table 58] Terminated Valid Calibration Points

VOH_{PU}, nom	ODT Value					
	240	120	80	60	48	40
VDDQ×0.5	VALID	VALID	VALID	VALID	VALID	VALID
VDDQ×0.6	DNU	VALID	DNU	VALID	DNU	DNU

NOTE :
1) Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.
2) If the VOH(nom) calibration point is changed, then re-calibration is required.
3) DNU = Do Not Use.

[Table 59] Pull-down Characteristics without ZQ Calibration

$R_{ONPD,NOM}$	Resistor	Vout	Min	Nom	Max	Unit	Notes
40.0Ω	R_{ON40PD}	0.5 × V_{OH}	0.70	1.00	1.30	$R_{ZQ/6}$	1
48.0Ω	R_{ON48PD}	0.5 × V_{OH}	0.70	1.00	1.30	$R_{ZQ/5}$	1

NOTE:
1) Across entire operating temperature range, without calibration.

13.0 ELECTRICAL CHARACTERISTICS AND AC TIMING

13.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR4X device.

13.1.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j\right) / N$$
$$where \qquad N = 200$$

Unit ‘tCK(avg)’ represents the actual clock average tCK(avg) of the input clock under operation. Unit ‘nCK’ represents one clock cycle of the input clock, counting the actual clock edges.
tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

13.1.2 Definition for tCK(abs)

t_{CK}(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.
t_{CK}(abs) is not subject to production test.

13.1.3 Definition for tCH(avg) and tCL(avg)

t_{CH}(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j\right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

t_{CL}(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j\right) / (N \times tCK(avg))$$
$$where \qquad N = 200$$

13.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
Both tCH(abs) and tCL(abs) are not subject to production test.

13.1.5 Definition for tJIT(per)

t_{JIT}(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).
t_{JIT}(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}.
t_{JIT}(per),$_{act}$ is the actual clock jitter for a given system.
t_{JIT}(per),$_{allowed}$ is the specified allowed clock period jitter.
t_{JIT}(per) is not subject to production test.

13.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

t_{JIT}(cc) = Max of |{tCK(i +1)- tCK(i)}|.

t_{JIT}(cc) defines the cycle to cycle jitter.

t_{JIT}(cc) is not subject to production test.

13.1.7 Definition for tERR(nper)

t_{ERR}(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).

t_{ERR}(nper)$,_{act}$ is the actual clock jitter over n cycles for a given system.

t_{ERR}(nper)$,_{allowed}$ is the specified allowed clock period jitter over n cycles.

t_{ERR}(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

t_{ERR}(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68 LN(n)) \times tJIT(per), min$$

t_{ERR}(nper),max can be calculated by the formula shown below

$$tERR(nper), max = (1 + 0.68 LN(n)) \times tJIT(per), max$$

Using these equations, t_{ERR}(nper) tables can be generated for each t_{JIT}(per),act value.

13.1.8 Definition for duty cycle jitter tJIT(duty)

t_{JIT}(duty) is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

$$tJIT(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

13.1.9 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

[Table 60] Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	t_{CK}(abs)	tCK(avg),min + tJIT(per),min	ps
Absolute Clock HIGH Pulse Width	t_{CH}(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	t_{CL}(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

NOTE :
1) tCK(avg),min is expressed is ps for this table.
2) tJIT(duty),min is a negative value.

13.2 Period Clock Jitter

LPDDR4X devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 13.4, AC Timing and how to determine cycle time de-rating and clock cycle de-rating.

13.2.1 Clock period jitter effects on core timing parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR4X device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

13.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

13.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

13.2.2 Clock jitter effects on Command/Address timing parameters

Command/address timing parameters (t_{IS}, t_{IH}, t_{ISb}, t_{IHb}) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/ CK_c) crossing. The specification values are not affected by the tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

13.2.3 Clock jitter effects on Read timing parameters

13.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,

if the measured jitter into a LPDDR4X device has tCK(avg) = 625ps, tJIT(per),act,min = -xx, and tJIT(per),act,max = +xx ps, then tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (xx - xx)/xx = yy tCK(avg).

13.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

13.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.

These parameters determine absolute Data-Valid window(DVW) at the LPDDR4X device pin.

Absolute min DVW @LPDDR4X device pin = min { (tQSH(abs)min – tDQSQmax), (tQSL(abs)min – tDQSQmax) }

This minimum DVW shall be met at the target frequency regardless of clock jitter.

13.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

13.2.4 Clock jitter effects on Write timing parameters

13.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

13.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

13.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into an LPDDR4X device has tCK(avg) = 625ps, tJIT(per),act,min = -xxps, and tJIT(per),act,max = +xx ps, then:

tDQSS,(min,derated) = 0.75 - (-xx + yy)/625 = xxxx tCK(avg)

tDQSS,(max,derated) = 1.25 - (xx . yy)/625 = xxxx tCK(avg)

13.3 LPDDR4X Refresh Requirement

[Table 61] LPDDR4X Refresh Requirement Parameters per die for Dual Channel SDRAM devices

Parameter		Symbol	16Gb	Unit
Density per Channel			8Gb	
Number of Banks per Channel			8	
Refresh Window Tcase ≤ 85°C		t_{REFW}	32	ms
Refresh Window 1/2-Rate Refresh		t_{REFW}	16	ms
Refresh Window 1/4-Rate Refresh		t_{REFW}	8	ms
Required number of REFRESH commands in a t_{REFW} window (min)		R	8,192	-
Average Refresh Internal	REFab	t_{REFI} 3)	3.904	us
	REFpb	t_{REFIpb}	488	ns
Refresh Cycle time (All Banks)		t_{RFCab}	280	ns
Refresh Cycle time (Per Bank)		t_{RFCpb}	140	ns
Per-bank Refresh to Per-bank Refresh different bank Time		$t_{pbR2pbR}$	90	ns

NOTE :

1) Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2) Self refresh abort feature is available for higher density devices starting with 12Gb dual channel device and 6Gb single channel device and tXSR_abort(min) is defined as tRFCpb + 17.5ns.
3) t_{REFI} values for all bank refresh is Tc = -25~85°C, Tc means Operating Case Temperature.

13.4 AC Timing

[Table 62] LPDDR4X AC Timing Table

Parameter	Symbol	Min/ Max	LPDDR4X			Unit
			3200Mbps	3733Mbps	4266Mbps	
Maximum clock frequency		~	1600	1866	2133	MHz
Clock Timing						
Average Clock Period	$t_{CK(avg)}$	MIN	0.625	0.536	0.468	ns
		MAX	100			
Average HIGH pulse width	$t_{CH(avg)}$[35]	MIN	0.45			t_{CK}(avg)
		MAX	0.55			
Average LOW pulse width	$t_{CL(avg)}$[35]	MIN	0.45			t_{CK}(avg)
		MAX	0.55			
Absolute clock period	$t_{CK(abs)}$	MIN	t_{CK}(avg) MIN + t_{JIT}(per) MIN			ns
Absolute HIGH clock pulse width	$t_{CH(abs)}$	MIN	0.43			t_{CK}(avg)
		MAX	0.57			
Absolute LOW clock pulse width	$t_{CL(abs)}$	MIN	0.43			t_{CK}(avg)
		MAX	0.57			
Clock period jitter	$t_{JIT(per)}$	MIN	-40	-36	-30	ps
		MAX	40	36	30	
Maximum Clock Jitter between two consecutive cycles	$t_{JIT(cc)}$	MAX	80	72	60	ps
Duty cycle jitter (with supported jitter)	$t_{JIT(duty)}$, allowed	MIN	min((t_{CH}(abs),min - t_{CH}(avg),min), (t_{CL}(abs),min - t_{CL}(avg),min)) × t_{CK}(avg)			ps
		MAX	max((t_{CH}(abs),max - t_{CH}(avg),max), (t_{CL}(abs),max - t_{CL}(avg),max)) × t_{CK}(avg)			
Core AC Parameters[17]						
READ latency (no DBI)	RL	MIN	28	32	36	t_{CK}(avg)
WRITE latency (set A)	WL	MIN	14	16	18	t_{CK}(avg)
ACTIVATE-to-ACTIVATE command period (same bank)	t_{RC}	MIN	t_{RAS} + t_{RPab} (with all-bank precharge) t_{RAS}+ t_{RPpb} (with per-bank precharge)			ns
Minimum Self-Refresh Time (Entry to Exit)	t_{SR}	MIN	max(15ns, 3tCK)			ns
SELF REFRESH exit to next valid command delay	t_{XSR}	MIN	Max (t_{RFCab} + 7.5ns, 2tCK)			ns
Exit power down to next valid command delay	t_{XP}	MIN	Max(7.5ns, 5tCK)			ns
CAS-to-CAS delay	t_{CCD}	MIN	BL/2			t_{CK}(avg)
CAS to CAS delay Masked Write	t_{CCDMW}[31]	MIN	4 × t_{CCD}			t_{CK}(avg)
Internal READ to PRECHARGE command delay	t_{RTP}	MIN	Max(7.5ns, 8tCK)			ns
RAS-to-CAS delay	t_{RCD}	MIN	Max (18ns, 4tCK)			ns
Row Precharge Time (single bank)	t_{RPpb}	MIN	Max (18ns, 4tCK)			ns
Row Precharge Time (all banks)	t_{RPab}	MIN	Max(21ns, 4tCK)			ns
Row active time	t_{RAS}	MIN	Max(42ns, 3tCK)			ns
		MAX	min (9 × t_{REFI} × Refresh Rate[19], 70.2)			us
WRITE recovery time	t_{WR}	MIN	Max(18ns, 6tCK)			ns
WRITE-to-READ delay	t_{WTR}	MIN	Max(10ns, 8tCK)			ns
Active bank-A to Active bank-B	t_{RRD}	MIN	Max(10ns, 4tCK)		Max (7.5ns, 4tCK)[32]	ns
Precharge to Precharge Delay	t_{PPD}[34]	MIN	4			tCK
Four-bank ACTIVATE Window	t_{FAW}	MIN	40		30[32]	ns
CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	t_{CKELPD}	MIN	Max(7.5ns, 3tCK)			ns

[Table 62] LPDDR4X AC Timing Table

Parameter	Symbol	Min/ Max	LPDDR4X			Unit
			3200Mbps	3733Mbps	4266Mbps	
READ AC Parameters 4)						
Read preamble	t_{RPRE} 5), 8)	MIN	2.0			t_{CK}(avg)
0.5 tCK Read postamble	t_{RPST} 5), 9)	MIN	0.5			t_{CK}(avg)
1.5 tCK Read postamble	t_{RPST}	MIN	1.5			t_{CK}(avg)
DQ low-impedance time from CK_t, CK_c	$t_{LZ(DQ)}$ 5)	MIN	(RL × t_{CK}) + $t_{DQSCK(Min)}$ - 200ps			ps
DQ high impedance time from CK_t, CK_c	$t_{HZ(DQ)}$ 5)	MAX	(RL × t_{CK}) + $t_{DQSCK(Max)}$ + $t_{DQSQ(Max)}$ + (BL/2 × t_{CK}) - 100ps			ps
DQS_c low-impedance time from CK_t, CK_c	$t_{LZ(DQS)}$ 5)	MIN	(RL × t_{CK}) + $t_{DQSCK(Min)}$ - ($t_{PRE(Max)}$ × t_{CK}) - 200ps			ps
DQS_c high impedance time from CK_t, CK_c	$t_{HZ(DQS)}$ 5)	MAX	(RL × t_{CK}) + $t_{DQSCK(Max)}$ + (BL/2 × t_{CK}) - (RPST(Max) × t_{CK}) - 100ps			ps
DQS-DQ skew	t_{DQSQ}	MAX	0.18			UI
tDQSCK AC Parameters						
DQS output access time from CK_t/CK_c	t_{DQSCK} 14)	MIN	1500			ps
		MAX	3500			
DQS output access time from CK_t/CK_c temperature variation	t_{DQSCK_temp} 15)	MAX	4			ps/°C
DQS output access time from CK_t/CK_c voltage variation	t_{DQSCK_volt} 16)	MAX	7			ps/mV
CK to DQS rank to rank variation	$t_{DQSCK\_rank2rank}$ 22), 23)	MAX	1.0			ns
Self Refresh Parameters						
Delay from SRE command to CKE Input low	t_{ESCKE} 24)	MIN	Max(1.75ns, 3tCK)			ns
Minimum Self Refresh Time	t_{SR} 24)	MIN	Max(15ns, 3tCK)			ns
Exit Self Refresh to Valid commands	t_{XSR} 24),25)	MIN	Max(tRFCab + 7.5ns, 2tCK)			ns
WRITE AC Parameters 4)						
Write command to 1st DQS latching	t_{DQSS}	MIN	0.75			t_{CK}(avg)
		MAX	1.25			
DQS input high-level width	t_{DQSH} 36)	MIN	0.4			t_{CK}(avg)
DQS input low-level width	t_{DQSL} 36)	MIN	0.4			t_{CK}(avg)
DQS falling edge to CK setup time	t_{DSS}	MIN	0.2			t_{CK}(avg)
DQS falling edge hold time from CK	t_{DSH}	MIN	0.2			t_{CK}(avg)
Write preamble	t_{WPRE}	MIN	2.0			t_{CK}(avg)
0.5 tCK Write postamble	t_{WPST} 21)	MIN	0.5			t_{CK}(avg)
1.5 tCK Write postamble	t_{WPST} 21)	MIN	1.5			t_{CK}(avg)
ZQ Calibration Parameters						
ZQ Calibration	t_{ZQCAL}	MIN	1			us
ZQ Calibration Values Latch Time	t_{ZQLAT}	MN	Max (30ns, 8tCK)			ns
ZQ Calibration RESET time	$t_{ZQRESET}$	MIN	Max (50ns, 3tCK)			ns
Power Down Parameters						
CKE minimum pulse width (HIGH and LOW pulse width)	t_{CKE}	MIN	max(7.5ns, 4tCK)			-
Delay from Valid command to CKE Input low	t_{CMDCKE} 26)	MIN	Max(1.75ns, 3tCK)			ns
Valid Clock Requirement after CKE Input Low	t_{CKELCK} 26)	MIN	Max(5ns, 5tCK)			ns
Valid CS Requirement before CKE Input Low	t_{CSCKE}	MIN	1.75			ns
Valid CS Requirement after CKE Input Low	t_{CKELCS}	MIN	Max(5ns,5tCK)			ns

[Table 62] LPDDR4X AC Timing Table

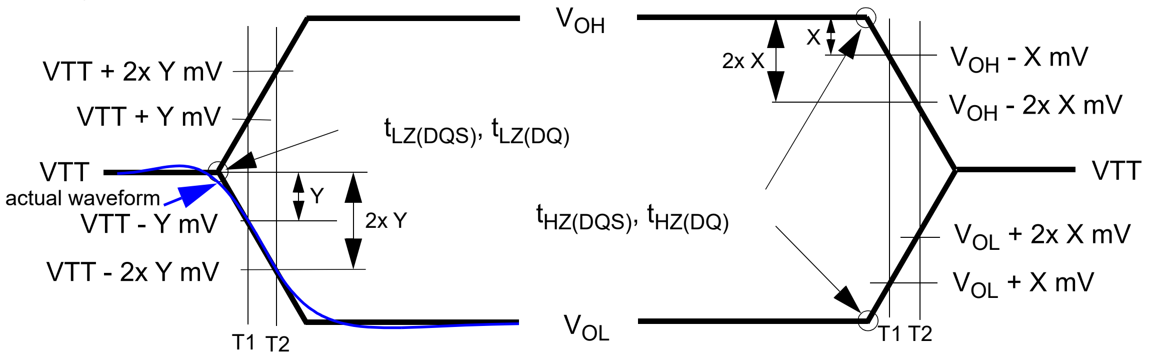
Parameter	Symbol	Min/ Max	LPDDR4X			Unit
			3200Mbps	3733Mbps	4266Mbps	
Valid Clock Requirement before CKE Input High	t_{CKCKEH} 26)	MIN	Max(1.75ns, 3tCK)			-ns
Exit power- down to next valid command delay	t_{XP} 26)	MIN	Max(7.5ns, 5tCK)			ns
Valid CS Requirement before CKE Input High	t_{CSCKEH}	MIN	1.75			ns
Valid CS Requirement after CKE Input High	t_{CKEHCS}	MIN	Max(7.5ns,5tCK)			ns
Valid Clock and CS Requirement after CKE Input low after MRW Command	$t_{MRWCKEL}$ 26)	MIN	Max(14ns,10tCK)			ns
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	t_{ZQCKE} 26)	MIN	Max(1.75ns,3tCK)			ns
Command Address Input Parameters 4)						
Rx Mask voltage - p-p	VcIVW	MAX	155	150	145	mV
Rx timing window	TcIVW	MAX	0.3			UI*
CA AC input pulse amplitude pk-pk	VIHL_AC	MIN	190	180	180	mV
CA input pulse width	TcIPW	MIN	0.6			UI*
Input Slew Rate over VcIVW	SRIN_cIVW	MIN	1			V/ns
		MAX	7			
Mode Register Read/Write AC Timing						
Additional time after tXP has expired until MRR command	t_{MRRI}	MIN	t_{RCD} + 3nCK			-
MODE REGISTER READ command period	t_{MRR}	MIN	8			nCK
MODE REGISTER WRITE command period	t_{MRW}	MIN	Max(10ns, 10nCK)			-
Mode register set command delay	t_{MRD}	MIN	Max(14ns, 10tCK)			-
Boot Parameters (10 MHz - 55 MHz) 11), 12), 13)						
Clock Cycle Time	t_{CKb}	max	100			ns
		MIN	18			
Address & Control Input Setup Time	t_{ISb}	MIN	1150			ps
Address & Control Input Hold Time	t_{IHb}	MIN	1150			ps
DQS Output Data Access Time from CK_t/CK_c	t_{DQSCKb}	MIN	2.0			ns
		MAX	10.0			
Data Strobe Edge to Output Data Edge	t_{DQSQb}	MAX	1.2			ns
Command Bus Training AC Parameters						
Valid Clock Requirement after CKE Input low	t_{CKELCK}	MIN	Max(5ns, 5nCK)			tCK
Data Setup for VREF Training Mode	$t_{DStrain}$	MIN	2			ns
Data Hold for VREF Training Mode	$t_{DHtrain}$	MIN	2			ns
Asynchronous Data Read	t_{ADR}	MAX	20			ns
CA Bus Training command to CA Bus Training command delay	t_{CACD} 29)	MIN	RU(t_{ADR}/t_{CK})			tCK
Valid Strobe Requirement before CKE Low	t_{DQSCKE} 30)	MIN	10			ns
First CA Bus Training Command Following CKE LOW	t_{CAENT}	MIN	250			ns
VREF Step Time-multiple steps	t_{VREFCA_LONG}	MAX	250			ns
VREF Step Time-one step	t_{VREFCA_SHORT}	MAX	80			ns
Valid Clock Requirement before CS High	$t_{CKPRECS}$	MIN	$2t_{CK} + t_{XP}$ (t_{XP} = max(7.5ns, 5nCK))			-
Valid Clock Requirement after CS High	$t_{CKPSTCS}$	MIN	max(7.5ns, 5nCK)			-
Minimum delay from CS to DQS toggle in command bus training	t_{CS_VREF}	MIN	2			tCK
Minimum delay from CKE High to Strobe High Impedance	$t_{CKEHDQS}$	-	10			ns
Valid Clock Requirement before CKE Input High	t_{CKCKEH}	MIN	Max(1.75ns, 3tCK)			
CA Bus Training CKE High to DQ Tri-state	t_{MRZ}	MIN	1.5			ns

[Table 62] LPDDR4X AC Timing Table

Parameter	Symbol	Min/ Max	LPDDR4X			Unit
			3200Mbps	3733Mbps	4266Mbps	
ODT turn-on Latency from CKE	$t_{CKELODTon}$	MIN	20			ns
ODT turn-off Latency from CKE	$t_{CKELODToff}$	MIN	20			ns
Exit Command Bus Training Mode to next valid command delay 33)	t_{XCBT_Short}	MIN	Max(5nCK, 200ns)			-
	t_{XCBT_Middle}	MIN	Max(5nCK, 200ns)			-
	t_{XCBT_Long}	MIN	Max(5nCK, 250ns)			-
Write Leveling Parameters						
DQS_t/DQS_c delay after write leveling mode is programmed	$t_{WLDQSEN}$	MIN	20			tCK
Write preamble for Write Leveling	t_{WLWPRE}	MIN	20			tCK
First DQS_t/DQS_c edge after write leveling mode is programmed	t_{WLMRD}	MIN	40			tCK
Write leveling output delay	t_{WLO}	MAX	20			ns
Mode register set command delay	t_{MRD}	MIN	Max(14ns, 10tCK)			ns
Valid Clock Requirement before DQS Toggle	$t_{CKPRDQS}$	MIN	Max(7.5ns, 4tCK)			-
Valid Clock Requirement after DQS Toggle	$t_{CKPSTDQS}$	MIN	Max(7.5ns, 4tCK)			-
Write leveling hold time	t_{WLH} 27)	MIN	75	60	50	ps
Write leveling setup time	t_{WLS} 27)	MIN	75	60	50	ps
Write leveling input valid window	t_{WLIVW} 28)	MIN	120	100	90	ps
Temperature De-Rating AC Timing 20)						
DQS output access time from CK_t/CK_c (derated)	t_{DQSCK}	MAX	3600			ps
RAS-to-CAS delay (derated)	t_{RCD}	MIN	t_{RCD} + 1.875			ns
ACTIVATE-to- ACTIVATE command period (derated)	t_{RC}	MIN	t_{RC} + 3.75			ns
Row active time (derated)	t_{RAS}	MIN	t_{RAS} + 1.875			ns
Row precharge time (derated)	t_{RP}	MIN	t_{RP} + 1.875			ns
Active bank A to active bank B (derated)	t_{RRD}	MIN	t_{RRD} + 1.875			ns

NOTE :

1) Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
2) All AC timings assume an input slew rate of TBDV/ns.
3) Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal VIX.
4) READ, WRITE, and Input setup and hold values are referenced to V_{REF}.
5) For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Operating and Timing [Burst Read:RL=12, BL=8, tDQSCK<tCK] shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
6) Output Transition Timing



Start driving point = 2 x T1 - T2   End driving point = 2 x T1 - T2

7) The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.
8) Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge. See Pre and Post-amble section in Operating & Timing spec
9) Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
10) Input set-up/hold time for signal (CA[9:0], CS).
11) To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b

appended (for example, tCK during boot is tCKb).
12) The LPDDR4X device will set some default values upon receiving a RESET (MRW) command as specified in “Definition”.
13) The output skew parameters are measured with default output impedance settings using the reference load.
14) Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
15) tDQSCK_temp max delay variation as a function of Temperature.
16) tDQSCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. t_{DQSCK_volt} should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage variation must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1-tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}.
17) Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
18) tXSR/tXP/tZQLAT are defined as “to the first rising clock edge next valid command”.
19) Refresh Rate is specified by MR4, OP[2:0].
20) Timing derating applies for operation at 85°C to 105°C.
21) The length of Write Postamble depends on MR3 OP1 setting.
22) The same voltage and temperature are applied to $t_{DQS2CK\_rank2rank}$.
23) $t_{DQSCK\_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
24) Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that t_{ESCKE} will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.

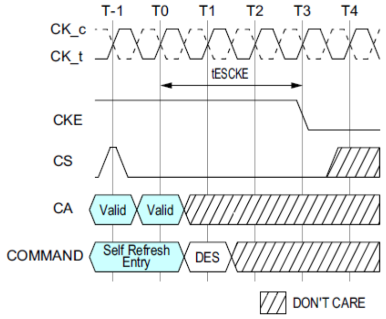


Figure 23. t_{ESCKE} Timing

25) MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.
26) Delay time has to satisfy both analog time(ns) and clock count(nCK). For example, t_{CMDCKE} will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.The case which 3nCK is applied to is shown below.

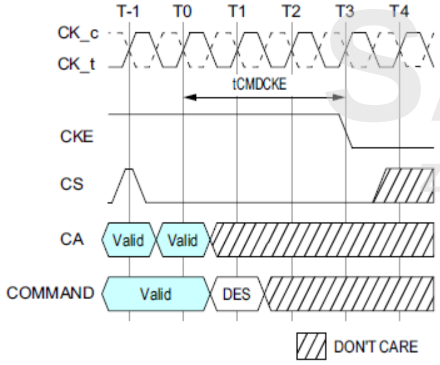


Figure 24. t_{CMDCKE} Timing

27) In addition to the traditional setup and hold time specifications above, there is value in a input valid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
28) t_{WLIVW} is defined in a similar manner to tdIVW_Total, except that here it is a DQS input valid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling input valid window. The DQS input mask for timing with respect to CK is shown in Figure 25. The "total" mask (tWLIVW) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

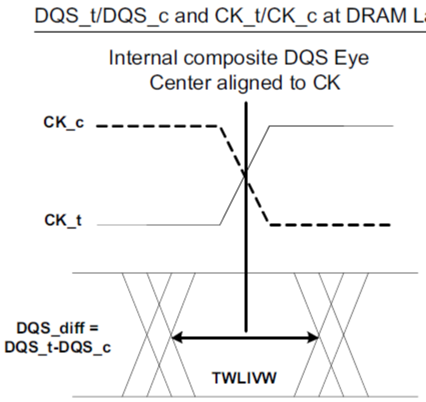


Figure 25. DQS_t/DQS_c to CK_t/CK_c timings at the DRAM pins referenced from the internal latch

29) If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
30) DQS_t has to retain a low level during t_{DQSCKE} period, as well as DQS_c has to retain a high level.
31) See Masked Write Operation for detail.

32) Devices supporting 4266Mbps specification shall support these timings at lower data rates.

33) Exit Command Bus Training Mode to next valid command delay Time depends on value of V_{REF}(CA) setting: MR12 OP[5:0] and V_{REF}(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally exit Command Bus Training Mode to next valid command delay Time may affect V_{REF}(DQ) setting. Settling time of V_{REF}(DQ) level is same as V_{REF}(CA) level.

34) Precharge to precharge timing restriction does not apply to Auto-Precharge commands.

35) This value is also valid for 1600Mbps Single-Ended CK ODT-off case.

36) This value is also valid for 1600Mbps Single-Ended WDQS ODT-off case.

13.5 CA Rx Voltage and Timing

The command and address(CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.
The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

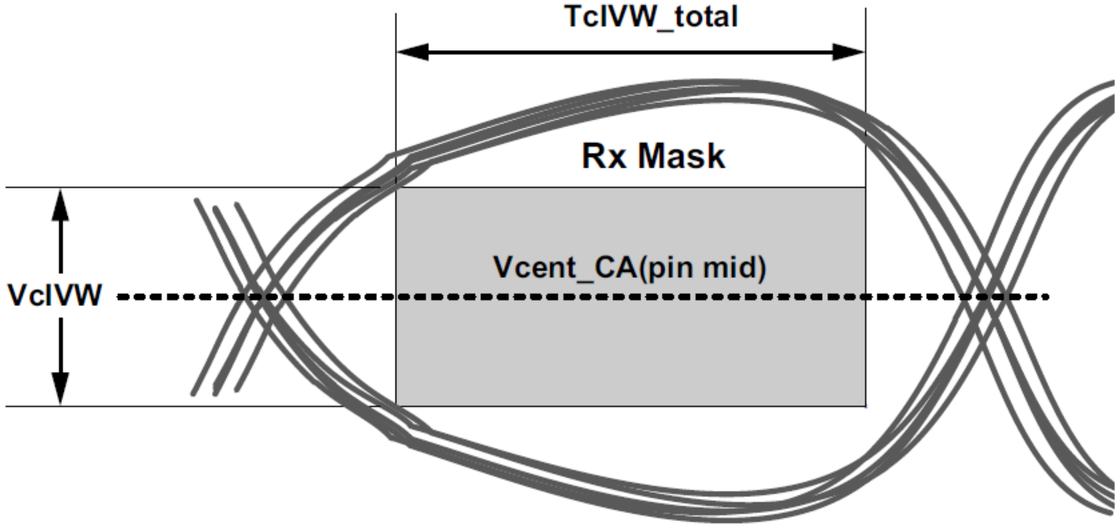


Figure 26. CA Receiver (Rx) mask

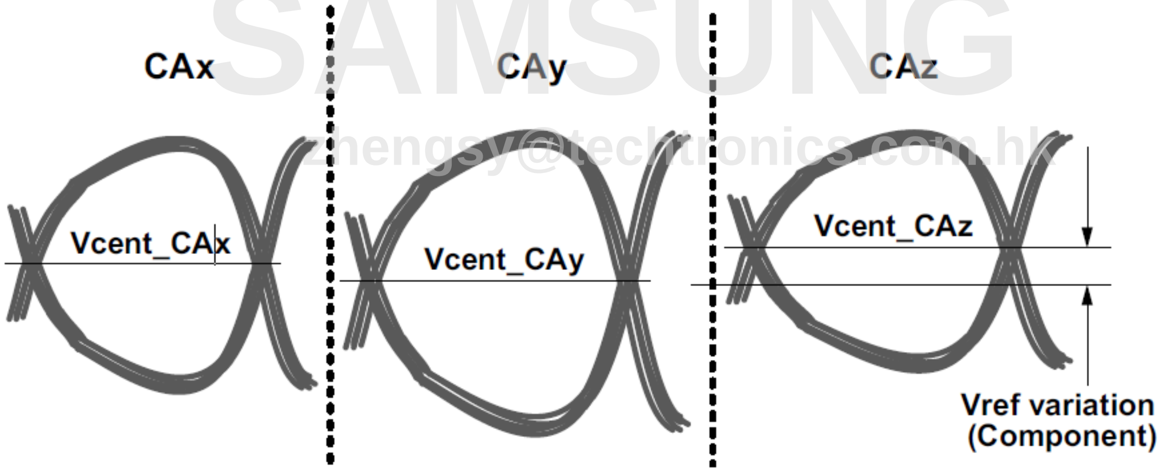
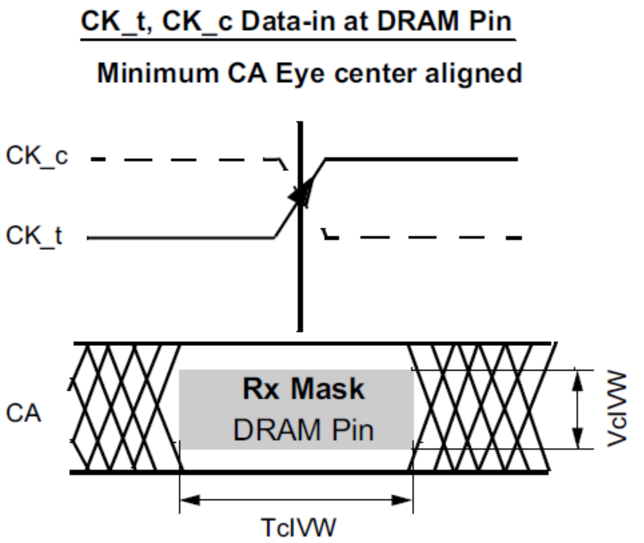


Figure 27. Across pin V_{REFCA} voltage variation

Vcent_CA(pin avg) is defined as the midpoint between the largest Vcent_CA voltage level and the smallest Vcent_CA voltage level across all CA and CS pins for a given DRAM component. Each CA Vcent level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 27. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.



TcIVW for all CA signals is defined as centered on the CK_t/CK_c crossing at the DRAM pin.

Figure 28. CA Timings at the DRAM pins

All of the timing terms in Figure 28. are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

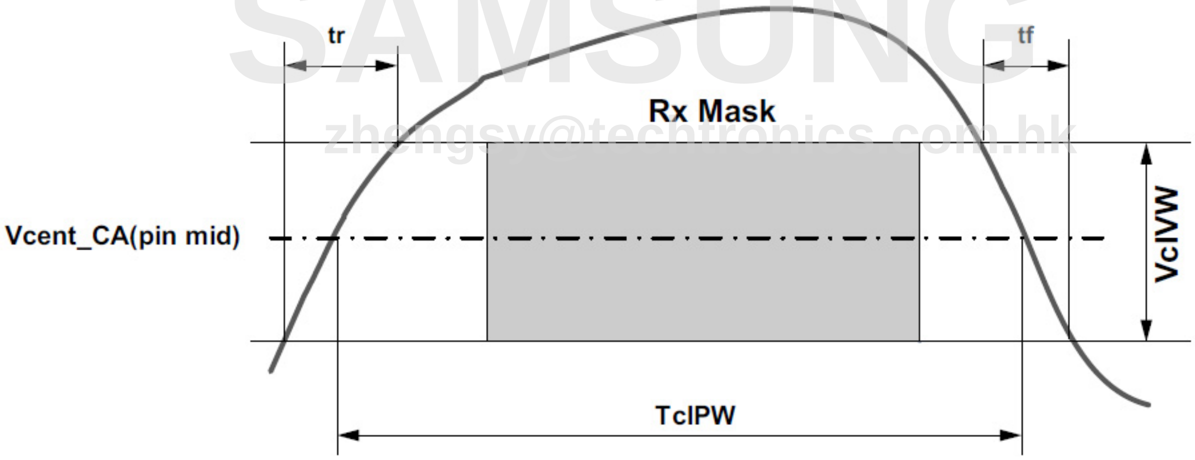


Figure 29. CA TcIPW and SRIN_cIVW definition (for each input pulse)

NOTE :
1) SRIN_cIVW=VcIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

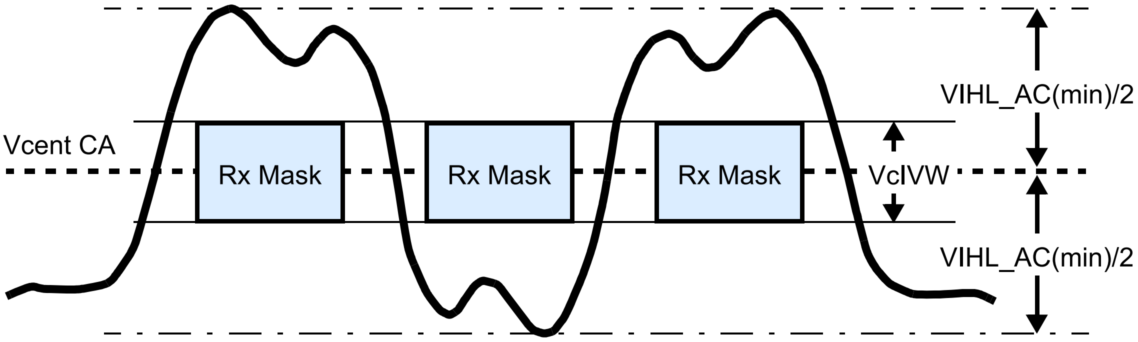


Figure 30. CA VIHL_AC definition (for each input pulse)

[Table 63] DRAM CMD/ADR, CS

Symbol	Parameter	DQ-1333 A)		DQ-1600				DQ-1866		DQ-3200		DQ-3733		DQ-4266		Unit	NOTE
				Clock SE 8)		Clock Diff. 9)											
		min	max	min	max	min	max	min	max	min	max	min	max	min	max		
VcIVW	Rx Mask voltage - p-p	-	175	-	220	-	175	-	175	-	155	-	150	-	145	mV	1,2,3
TcIVW	Rx timing window	-	0.3	-	0.35	-	0.3	-	0.3	-	0.3	-	0.3	-	0.3	UI*	1,2,3
VIHL_AC	CA AC input pulse amplitude pk-pk	210	-	210	-	210	-	210	-	190	-	180	-	180	-	mV	4,7
TcIPW	CA input pulse width	0.55	-	0.55	-	055	-	0.55	-	0.6	-	0.6	-	0.6	-	UI*	5
SRIN_-cIVW	Input Slew Rate over VcIVW	1	7	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	6

*** UI=tCK(avg)min**

NOTE :

1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2) Rx mask voltage VcIVW total(max) must be centered around Vcent_CA (pin_mid).
3) Vcent_CA must be within the adjustment range of the CA internal Vref.
4) CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5) CA only minimum input pulse width defined at the Vcent_CA (pin mid).
6) Input slew rate over VcIVW Mask centered at Vcent_CA (pin mid).
7) VIHL_AC does not have to be met when no transitions are occurring.
8) MR51 OP[3] = 1B: Single ended Clock, Only CK_t.
9) MR51 OP[3] = 0B: Differential Clock (Default), CK_t /CK_c.

A) The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

13.6 DRAM Data Timing

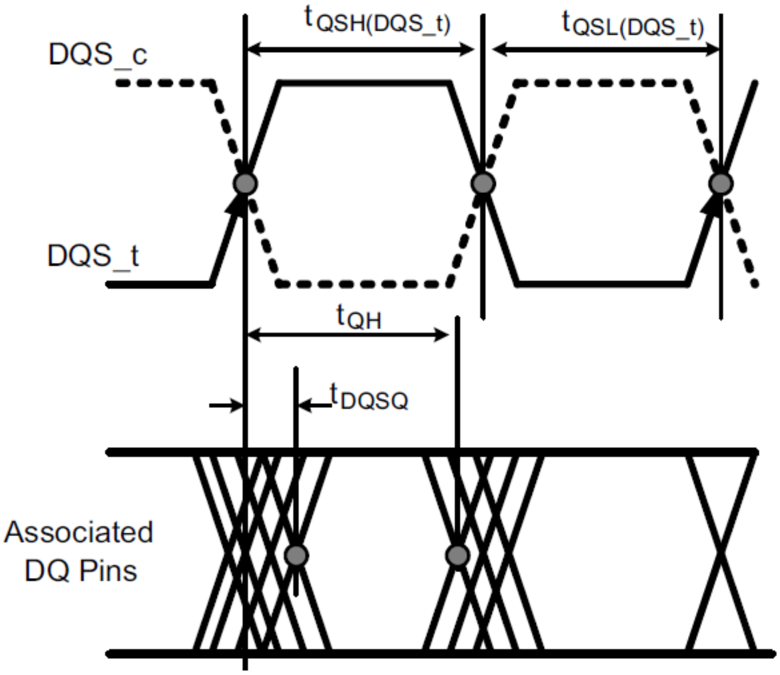


Figure 31. Read data timing definitions tQH and tDQSQ across on DQ signals per DQS group

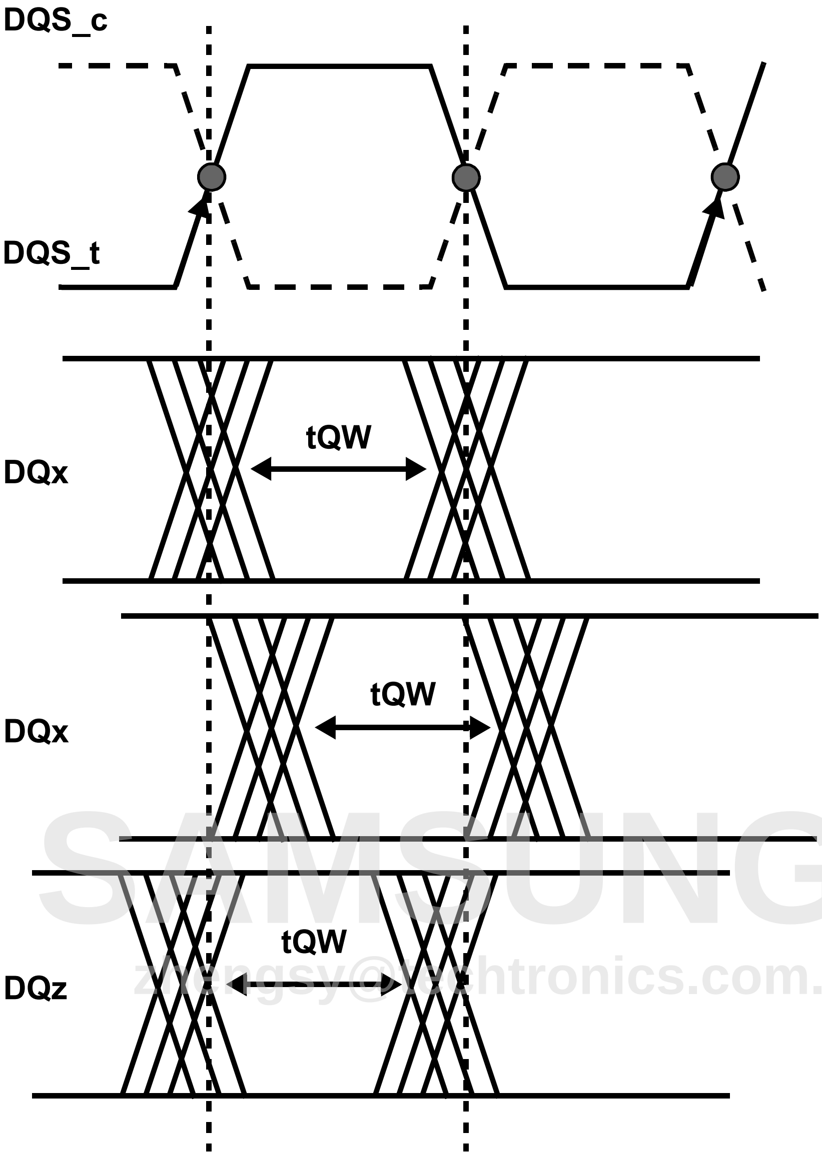


Figure 32. Read data timing tQW valid window defined per DQ signal

[Table 64] Read output timings

Parameter	Symbol	LPDDR4X-1600/1866		LPDDR4X-2133/2400		LPDDR4X-3200		LPDDR4X-3733		LPDDR4X-4266		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Data Timing													
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Disabled)	t_{DQSQ}	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	t_{QH}	$\min(t_{QSH}, t_{QSL})$	-	$\min(t_{QSH}, t_{QSL})$	-	$\min(t_{QSH}, t_{QSL})$	-	$\min(t_{QSH}, t_{QSL})$	-	$\min(t_{QSH}, t_{QSL})$	-	UI	
DQ output window time total, per pin (DBI-Disabled)	t_{QW_total}	0.75	-	0.73	-	0.7	-	0.7	-	0.7	-	UI	3
DQ output window time deterministic, per pin (DBI-Disabled)	t_{QW_dj}	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI	2,3
DQS_t, DQS_c to DQ Skew total, per group, per access (DBI-Enabled)	t_{DQSQ_DBI}	-	0.18	-	0.18	-	0.18	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	t_{QH_DBI}	$\min(t_{QSH\_DBI}, t_{QSL\_DBI})$	-	$\min(t_{QSH\_DBI}, t_{QSL\_DBI})$	-	$\min(t_{QSH\_DBI}, t_{QSL\_DBI})$	-	$\min(t_{QSH\_DBI}, t_{QSL\_DBI})$	-	$\min(t_{QSH\_DBI}, t_{QSL\_DBI})$	-	UI	
DQ output window time total, per pin (DBI-Enabled)	$t_{QW\_total\_DBI}$	0.75	-	0.73	-	0.7	-	0.7	-	0.7	-	UI	3
Data Strobe Timing													
DQS_t, DQS_c differential output low time (DBI-Disabled)	t_{QSL}	$t_{CL(abs)}$ -0.05	-	$t_{CL(abs)}$ -0.05	-	$t_{CL(abs)}$ -0.05	-	$t_{CL(abs)}$ -0.05	-	$t_{CL(abs)}$ -0.05	-	$t_{CK(avg)}$	3,4
DQS_t, DQS_c differential output high time (DBI-Disabled)	t_{QSH}	$t_{CH(abs)}$ -0.05	-	$t_{CH(abs)}$ -0.05	-	$t_{CH(abs)}$ -0.05	-	$t_{CH(abs)}$ -0.05	-	$t_{CH(abs)}$ -0.05	-	$t_{CK(avg)}$	3,5
DQS_t, DQS_c differential output low time (DBI-Enabled)	t_{QSL_DBI}	$t_{CL(abs)}$ -0.045	-	$t_{CL(abs)}$ -0.045	-	$t_{CL(abs)}$ -0.045	-	$t_{CL(abs)}$ -0.045	-	$t_{CL(abs)}$ -0.045	-	$t_{CK(avg)}$	4,6
DQS_t, DQS_c differential output high time (DBI-Enabled)	t_{QSH_DBI}	$t_{CH(abs)}$ -0.045	-	$t_{CH(abs)}$ -0.045	-	$t_{CH(abs)}$ -0.045	-	$t_{CH(abs)}$ -0.045	-	$t_{CH(abs)}$ -0.045	-	$t_{CK(avg)}$	5,6

***Unit UI = tCK(avg)min/2**

NOTE :

1) The deterministic component of the total timing. Measurement method tbd.
2) This parameter will be characterized and guaranteed by design.
3) This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
4) tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5) tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6) This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

13.7 DQ Rx Voltage And Timing

The DQ input receiver mask for voltage and timing is shown Figure 33. is applied per pin. The “total” mask (VdIVW_total, TdiVW_total) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

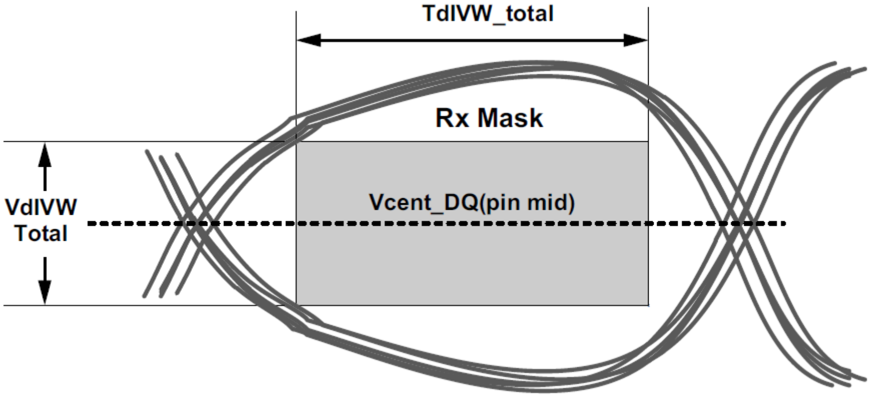


Figure 33. DQ Receiver (Rx) mask

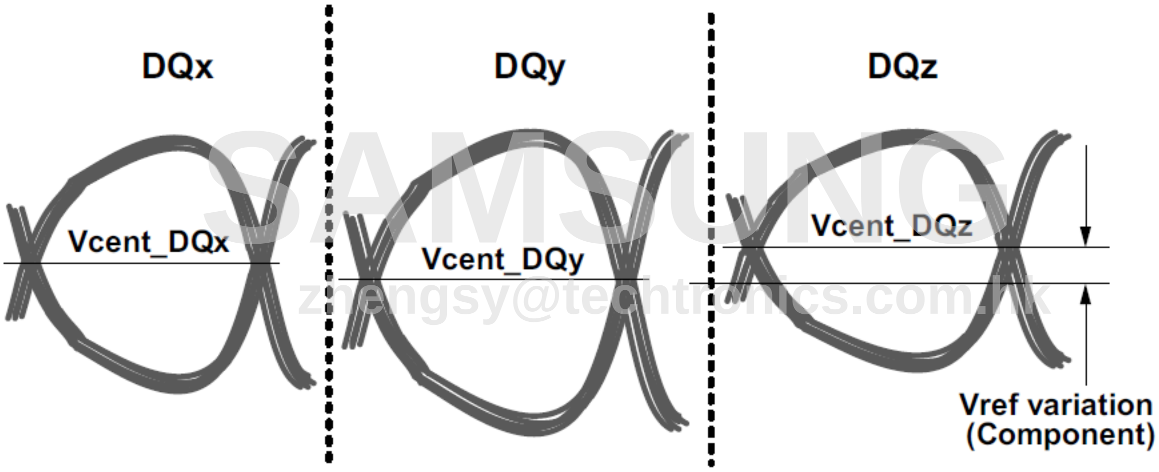


Figure 34. Across pin V_{REF}DQ voltage variation

Vcent_DQ(pin mid) is defined as the midpoint between the largest Vcent_DQ voltage level and the smallest Vcent_DQ voltage level across all DQ pins for a given DRAM component. Each DQ Vcent is defined by the center, i.e., widest opening, of the cumulative data input eye as depicted in Figure 34. This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level Vref will be set by the system to account for Ron and ODT settings.

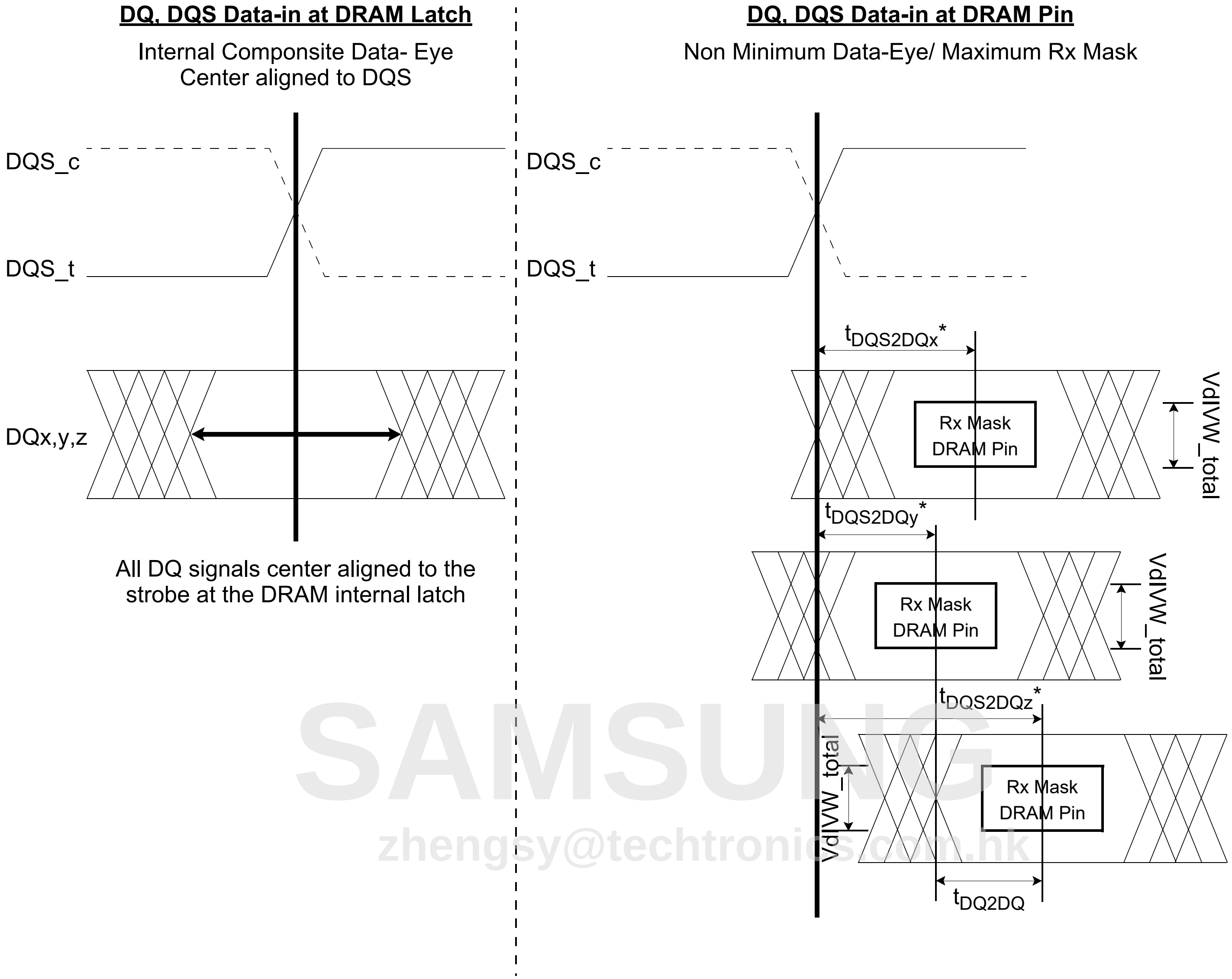


Figure 35. DQ to DQS t_{DQS2DQ} & t_{DQDQ} Timings at the DRAM pins referenced from the internal latch

NOTE :

1) t_{DQS2DQ} is measured at the center(midpoint) of the TdiVW window.
2) DQz represents the max t_{DQS2DQ} in this example.
3) DQy represents the min t_{DQS2DQ} in this example.

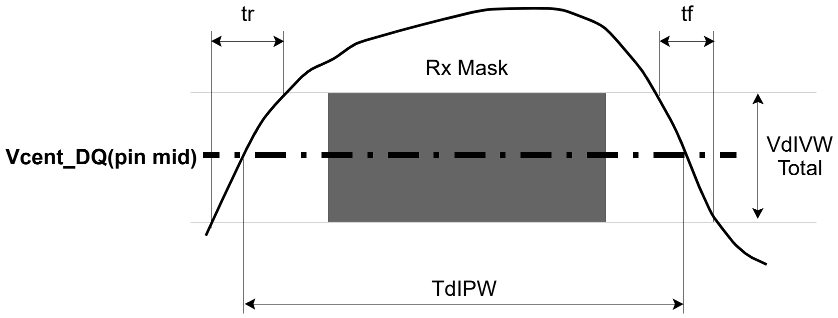


Figure 36. DQ TdIPW and SRIN_dIVW definition (for each input pulse)

NOTE :
1) SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

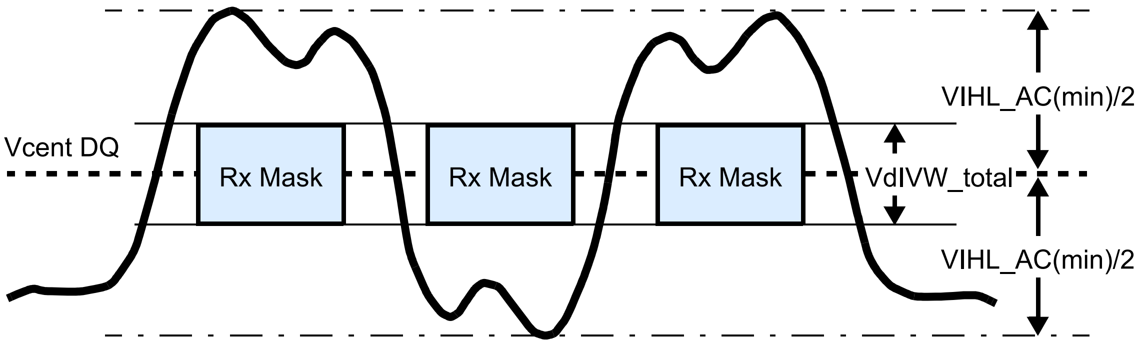


Figure 37. DQ VIHL_AC definition (for each input pulse)

[Table 65] DRAM DQs In Receive Mode;

Symbol	Parameter	1600 [A]				18662133/ 2400		3200		3733		4266		Unit	NOTE
		WDQS SE[17]		WDQS Diff[18]											
		min	max	min	max	min	max	min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	180	-	140	-	140	-	140	-	130	-	120	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.35	-	0.22	-	0.22	-	0.25	-	0.25	-	0.25	UI*	1,2,4
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	-	TBD	UI*	1,2,4,12
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	180	-	180	-	180	-	170	-	mV	5,13
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	0.45	-	UI*	6
t_{DQS2DQ}	DQ to DQS offset	250	700	250	700	250	700	250	700	250	700	250	700	ps	7
t_{DQ2DQ}	DQ to DQ offset	-	30	-	30	-	30	-	30	-	30	-	30	ps	8
t_{DQS2DQ_temp}	DQ to DQS offset temperature variation	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	-	0.4	ps/°C	9
t_{DQS2DQ_volt}	DQ to DQS offset voltage variation	-	25	-	25	-	25	-	25	-	25	-	25	ps/ 50mV	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	1	7	1	7	1	7	1	7	1	7	1	7	V/ns	11
$t_{DQS2DQ\_rank2rank}$	DQ to DQS offset rank to rank variation	-	200	-	200	-	200	-	200	-	200	-	200	ps	14,15,16

*** UI=tck(avg)min/2**

NOTE :

1) Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2) The design specification is a BER <tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3) Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4) Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5) DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ
6) DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7) DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation
8) DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9) TDQS2DQ max delay variation as a function of temperature.
10) TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package.
11) Input slew rate over VdIVW Mask centered at Vcent_DQ(pin mid).
12) Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13) VIHL_AC does not have to be met when no transitions are occurring.
14) The same voltage and temperature are applied to $t_{DQS2DQ\_rank2rank}$.
15) $t_{DQS2DQ\_rank2rank}$ parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
16) $t_{DQS2DQ\_rabk2rank}$ support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.
17) MR51 OP[2]=1B : Single ended Write DQS.
18) MR51 OP[2]=0B : Differential Write DQS.

A) The Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example TdIVW_total(ps) = 137.5ps at or below 1600 operating frequencies.